**Verification of Analog Circuits**

- **Motivation**
  - Up to 70% of the design time is taken by verification issues
  - Verification of analog signals (continuous in time and value) is very time consuming

- **Goal**
  - Development of basic elements of an integrated methodology for verification of analog circuits
  - To verify the applicability of the methods for an industrial assignment
  - **Scientific and technical goals**
    - Development of methods and rules for the creation of models which can be simulated quickly and also sufficiently describe many physical effects (e.g. mixed discipline or temperature).
    - Investigation and development of formal verification methods for analog circuits, i.e. model checking + equivalence checking.
    - Development of methods for assertion-based verification, and of formal procedures for performance and tolerance verification.
    - Implementation of an integrated methodology for multilevel verification of analog systems considering mixed-signal/mixed-domain aspects and using the aforementioned points.

- **Expected economical benefit**
  - Increase the verification efficiency by minimum 30% 
  - Reduce the number of redesigns by 20%
  - Improve the product quality

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**Verification oriented modeling**

- **Simulation performance**
  - Examination of modeling approaches and simulation algorithms
  - Reduction of simulation time by optimized behavioral models with sufficient accuracy

- **Verification oriented modeling for very high temperatures**
  - Determination of the behavior of power transistors at very high temperatures (300°C)
  - Adoption of the transistor model for the verification at very high temperatures

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**Formalized verification**

- **Model checking**
  - Investigation and development of model checking algorithms for analog circuits
  - Development of a suitable specification language for analog circuits

- **Equivalence checking**
  - Investigation and development of equivalence checking algorithms for two analog circuits and models respectively
  - Determination of requirements for behavioral modeling

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**Multi level verification**

- **Application-oriented verification of complete ICs**
  - Development of efficient task and application specific verification strategies on block level and for complete ICs
  - As possible a complete verification coverage

- **System level co-simulation**
  - Development of methods to accelerate the verification on system level by co-simulation
  - Consideration of different abstraction levels
  - Application of different languages/simulators
  - Mapping of analog circuit parts in programmable hardware and coupling of this hardware with AMS simulators

- **Application of models across abstraction levels**
  - Development of methods for functional circuit test across all abstraction levels
  - Consideration of process and operational tolerances on different abstraction levels