MunEDA | DESIGN AUTOMATION CONFERENCE 54 | Empowering Innovation

MunEDA @ DAC Design Automation Conference - Austin 2017

Dear MunEDA Friends & Users,

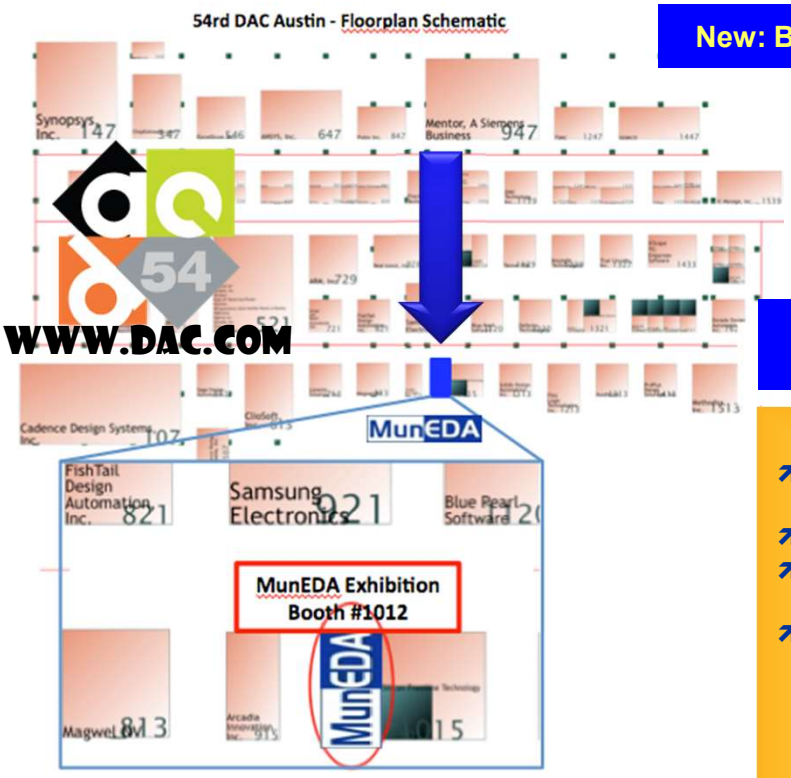
We are pleased to invite you to visit our MunEDA booth and workshops at 54rd DAC Exhibition, Mon-Wed June 19-21 2017 Austin, TX (www.dac.com).

MunEDA booth # 1012 in main exhibition hall

Circuit Schematic Migration & IP Porting
Learn more...

Variation Analysis, PVT, Monte Carlo & High-Sigma
Learn more...

Circuit Sizing for Low Power, Yield & Reliability
Learn more...



New: BTI-induced SRAM Bitcell Optimization

For arranging a meeting with MunEDA at DAC 2017 please contact us with:

info@muneda.com

New: Circuit Optimization for Radiation Hardening

MunEDA News at DAC 2017

- Advances in Custom Circuit Design Migration and IP Porting
- Low-Power Optimization of Custom IC Designs
- BTI Induced Dispersion: Challenges for SRAM Bit Cell Optimization
- Efficient and accurate high sigma analysis and optimization for
  - Memory I/O
  - Standard cells
  - SRAM bitcell, sensing, control including hierarchical large circuit analysis
- PCM targeting for debugging yield issues
- Full Custom Design for Reliability, Aging & Radiation Hardening

MunEDA DAC Special Topic: Low Power Circuit Sizing for IoT

- **Why is multi-objective automated circuit sizing challenging for IoT designs.**
- **How can MunEDA automated sizing tools be leveraged to achieve high-performance and reliable to IoT designs.**
- **How are statistices incorporated into sizing to consider device mismatch and process centering.**
- **What is the technology behind the MunEDA automated sizing environment – with enouth math/statistics to be interesting but not overwhelming.**
- **How can MunEDA sensitivity-based tools be useful to test and confirm and validate current intuition of my IoT designs**

Ask for our special introduction Low Power Circuit Sizing for IoT, info@muneda.com

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See you all in Austin for 2017 MunEDA DAC Exhibition and Workshops – www.muneda.com