# DATE 2006 Special Session: DFM/DFY Design for Manufacturability and Yield - influence of process variations in digital, analog and mixed-signal circuit design

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## Abstract

The concepts of Design for Manufacturability and Design for Yield DFM/DFY are bringing together domains that co-existed mostly separated until now – circuit design, physical design and manufacturing process. New requirements like SoC, mixed analog/digital design and deep-submicron technologies force to a mutual integration of all levels. A major challenge coming with new deep-submicron technologies is to design and verify integrated circuits for high yield. Random and systematic defects as well as parametric process variations have a large influence on quality and yield of the designed and manufactured circuits. With further shrinking of process technology, the on-chip variation is getting worse for each technology node. For technologies larger than 180nm feature sizes, variations are mostly in a range of below 10%. Here an acceptable yield range is achieved by regular but error-prone re-shifts of the drifting process. However, shrinking technologies down to 90nm, 65nm and below cause on-chip variations of more than 50%. It is understandable that tuning the technology process alone is not enough to guarantee sufficient yield and robustness levels any more. Redesigns and, therefore, respins of the whole development and manufacturing chain lead to high costs of multiple manufacturing runs. All together the risk to miss the given market window is extremely high. Thus, it becomes inevitable to have a seamless DFM/DFY concept realized for the design phase of digital, analog, and mixed-signal circuits. New DFY methodologies are coming up for parametric yield analysis and optimization and have recently been made available for the industrial design of individual analog blocks on transistor level up to 1500 transistors. The transfer of yield analysis and yield optimization techniques to other abstraction levels – both for digital as well as for analog – is a big challenge. Yield analysis and optimization is currently applied to individual circuit blocks and not to the overall chip yielding on the one hand often too pessimistic results - best/worst case and OCV (On Chip Variation) factor - for the digital parts. On the other hand for analog often very high efforts are spent to design individual blocks with high robustness (>6σ). For abstraction to higher digital levels first approaches like statistical static timing analysis (SSTA) are under development. For the analog parts a strategy to develop macro models and hierarchical simulation or behavioral simulation methodologies is required that includes low-level statistical effects caused by local and global process variation of the individual devices.

## 1. VLSI Design for Yield on Chip Level *(M. Bühler, J. Koehl, J. Bickford, J. Hibbeler)*

Today's shrinking feature sizes allow the integration of several hundred million transistors on a single chip and even a billion transistor chip no longer seems to be a vision of the distant future. The increasing number of transistors and decreasing feature size add design complexity and make producing acceptable yields challenging. Yield loss caused by the well known opens and shorts mechanism, parametric variation sensitivity, and the sheer number of devices add complexity to the physical design so that the simple worst-case/best-case sign off is no longer sufficient to ensure functionality. With these challenges, design for yield (DFY) and design for manufacturing (DFM) become even more important design goals.

Wire spreading and redundant via insertion (see *Figure 1*) **[1]** are two DFY/DFM approaches widely used in current chip-level physical design. Both were implemented to mitigate yield loss in aluminium technologies where wire-level shorts and via opens were the major yield detractors. Newer copper technologies exhibit increased sensitivity to metal opens. Wiring opens are now at least as important as shorts. Since wire spreading increases sensitivity to metal opens by adding additional wire length as it separates the wires, use of this technique does not

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always result in yield improvement. Wire widening and non-tree routing **[2]** with redundant paths are promising extensions of wire-spreading concepts that allow optimization for yield in copper technologies.

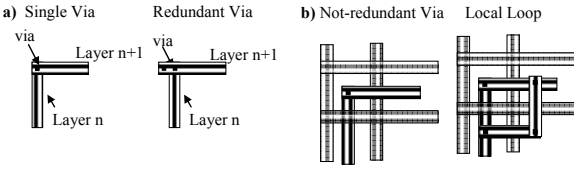


*Figure 1: Redundant via and local loops*

Copper technologies exhibit increased sensitivity to via opens. High via resistance in these technologies can significantly degrade critical signal timing. Use of redundant via insertion (creation of a second via in close proximity to the original via) typically results in via redundancy of 60-80%. These rates are no longer sufficient to meet yield objectives. Local loops **[3]** provide a means of improving redundancy through the use of a short loop (figure 1b) rather than currently used redundant vias. Use of loops can reduce the number of nonredundant vias by 70-80% and reduce sensitivity to cluster defects (cluster defects are known to block both the original and the doubled via created using current via redundancy techniques). Application of the before-mentioned yield optimization techniques in 65nm and 45nm technologies provides new challenges.

Maximizing yield requires trade-offs between wire length, wire spacing, and the number of vias. While it is desirable to minimize wirelength, maximize wire spacing, and minimize the number of vias, optimizing any one, results in overall chip yield sub-optimization. Layout practices need to consider the relative sensitivity in the target technology to metal shorts, metal opens, and via opens. Information on the mechanism causing the fail as well as overall yield information is needed so that layout practices can be optimized. New extended test methodology and statistical evaluation have recently been proposed **[4]**.

To make the best yield / performance / power trade-off, accurate yield estimation is needed throughout the physical design process. State-of-the-art Critical Area Analysis (CAA) is typically used for yield estimation **[5]**, but CAA has several drawbacks:

1. CAA runs are compute intensive, making it expensive and time consuming to run CAA on many design alternatives.
2. CAA identifies global failure rates, but doesn't identify specific locations that designers could consider modifying.
3. The global nature of CAA make it of limited use to define interaction between product yield and physical design tool settings.
4. CAA identifies only random yield sensitivities. CAA does not provide a means of estimating yield loss caused by systematic defects.

Application of CAA to individual library elements used in a cell-based library combined with integration of this information provides a novel technique to minimize drawbacks 1 and 3. This technique can provide a quick yield estimate for a given design as well as a means to optimize layout tools to trade yield for power and performance through the choice of several logically equivalent cells in a cell library.

Use of expert systems to model systematic yield loss **[6]** provides a way to address item 4. Mechanisms creating yield loss in a technology are identified and the layout is checked for such structures. Feedback provided to designers helps to optimize the layout against systematic defects. Since models to predict systematic yield loss do not exist, systematic defect sensitivity cannot be included in design cost trade-offs.

Nanometer technologies provide many new process features that require additional processing (example: additional VT offerings). In past technologies, across chip line-width variation (ACLV) was characterized and monitored, as part of the certification of design systems, but chip layout constraints to manage ACLV were not implemented. In 65nm and 45nm technologies, smaller feature sizes, higher circuit density, additional VT offerings, and more metal levels increase sensitivity to parametric fails. Modification of layout techniques may be needed to meet these new challenges.

Variation Aware Timing **[7]** and Statistical Timing **[8]** are techniques that allow parametric sensitivity optimization in designs. The following item addresses this subject in detail.

## 2. Statistical Design for Digital Circuits: Statistical Static Timing Analysis (SSTA) *(U. Schlichtmann)*

### 2.1 Variations are increasing

In digital design, traditionally we have dealt with variations in the manufacturing process by guard-banding generously against them, using a corner-based design approach. This approach identifies "parameter corners", typically such that $3\sigma$ of all manufactured circuits will not exceed these corner values. It assumes that variations exist between

different dies, but that within one die components such as transistors behave identical. This paradigm is breaking down. Manufacturing variations are increasing relative to their nominal values, and new process technologies result in much less benefit regarding performance and power consumption than was the case in the past, so generous guardbanding based on 3σ corners is not acceptable anymore. At the same time, variations within the same die (WID variations) are increasing significantly (Fig. 2). These variations cannot be handled at all by the existing corner-based methodologies.

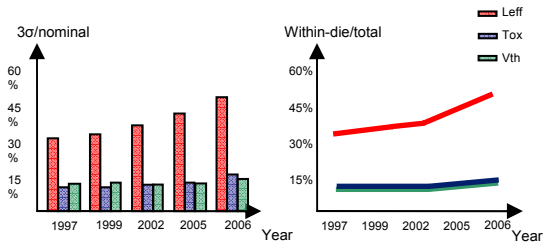


*Figure 2: Process Variation Trends [9]*

Currently, designers in advanced process technologies deal with these effects by enhancing traditional corner-based static timing analysis (STA) by on-chip variation (OCV) factors, or by increasing the number of process corners. These concepts do not capture the statistical nature of the WID variations very well, however.

Design trends recently have aggravated the problem of WID variations. Some of these variation sources, such as dopant fluctuations, are purely random in nature. Their relative effect decreases with the number of logic stages in a path. The trend in design, however, has been to reduce the number of logic stages between registers, in order to increase the clock frequency. Also, traditional STA-based design optimization tends to create a large number of critical paths that have a delay just slightly below the maximum permissible path delay. If statistical considerations are taken into account, the variation of the actual delay distribution increases with the number of critical paths.

Statistical design for digital circuits is a promising new approach to handle increasing process variations, especially WID variations. The goal is to treat these variations, which are statistical in nature, actually as statistical quantities during design. This approach will allow a more accurate description, eliminating the need for broad guardbanding. Sensitivities will be identified properly and can be optimized. Initially, the focus will be on statistical analysis (Statistical Static Timing Analysis, SSTA). Based on analysis, statistical optimization methods will follow.

## 2.2 Key challenges for SSTA

Key challenges in developing an SSTA tool are as follows:

- Delay modeling for cells and interconnect. While most process variations can be described by normal distributions, this is not necessarily the case for the delay variations caused by these process variations. To simplify calculations, most approaches proposed so far assume a linear dependency of delay on process variations (and thus a normal distribution) **[8, 10]**. Recently, higher order models have appeared **[11, 12]**. Analytical modeling of gate-level behavior appears to be a promising alternative, but has not received much attention yet.
- Propagation of delay distribution through a circuit. After the delay distribution of all circuit components has been modeled, the delay of an entire circuit needs to be determined. Essential required operations are the SUM of random variables, and the MAX/MIN of random variables. Especially for MAX/MIN, it is computationally expensive to determine the result exactly. Most proposed approaches therefore make the assumption that the results of these operations are normal distributed. Also, correlations e.g. between different gates need to be considered – resulting either from reconvergence in the circuit or from spatial relations **[13, 10]**.
- Integration of SSTA into the design flow. Two different basic approaches are to compute the delay distribution in path-based **[14]** or block-based **[8]** manner. These approaches differ in accuracy and computational complexity. For path-based approaches it has been proposed to run a traditional STA first, and then analyze only the n most critical paths accurately using SSTA, due to the high computational effort. The risk is, however, that the statistically most critical path is missed. Block-based approaches suffer from a lack of accuracy especially for the MAX/MIN operation.
- An SSTA design methodology will require at-speed testing of manufactured circuits. While this has traditionally been done for µPs, ASICs have relied more on purely structural test. The determination of cost-efficient at-speed tests for ASICs has not received much attention yet.

### 2.3 Industrial applicability and Outlook

First SSTA approaches are already being used in industry. Their accuracy is not fully clear yet, however. Comparisons to Monte-Carlo simulations that are typically presented in the literature usually employ gate-level timing models incorporating some of the same assumptions used in SSTA. Furthermore, the dependency of delay on slope and load has not received significant attention in the literature on SSTA yet.

Traditional STA required over a decade to move from first academic proposals to broad industry adoption. As well, algorithms for optimization of analog circuits based on statistical descriptions of process variations **[17]** took at least a decade to achieve meaningful industrial usage. It remains to be seen how long the process of widespread industrial adoption will take for SSTA.

In addition to research on improved and enhanced SSTA, researchers are increasingly turning their attention to statistical optimization rather than just analysis. First promising approaches have been presented, but the topic is still in its infancy.

## 3. Focussing Design for Yield DFY concepts for analog and mixed-signal circuits *(M. Pronath, A. Ripp)*

Design for Yield concepts are mostly focusing on the analog and mixed-signal part of a circuit that concentrates especially on the front-end design process based on simulating, analyzing and optimizing circuit topologies. In the world of analog and mixed-signal the sizing step, i.e. finding values for all circuit elements of a chosen topology, is one of the most critical tasks in the design phase.

Especially for new technology nodes such as 90nm and 65nm statistical and operating parameters play an essential role for robustness and performance of integrated circuits. As a consequence all of these dependencies and influences have to be taken into account when adjusting the values for the design parameters in order to ensure the functionality of the circuit. In the critical RF, analog, and mixed-signal design flows the designer needs new guidelines and tools to deal with all these multiple factors impacting yield and performance. It is essential to have yield optimization with built-in sensitivity analysis that derives how process parameters influence the performance of a design. Apparently this has large effects in increasing design efficiency, overall-cost and time-to-market. Three main reasons for missing yield goals and market windows caused by analog/mixed-signal designs are essential: design process, process technology and design complexity.

The industry today is confronted especially with short product cycles, a shortage of design resources and automation skills. Rapid technology changes as well as increasing influence of parameter variations on the circuit robustness are main issues on the process technology side. Both digital and analog circuits today are manufactured on one single chip using process technologies originally designed for the digital world only. This has large influence on functionality and robustness of the whole chip, because analog circuits strongly depend on a combination of topology, performances, sizing and technology. Conventional design methodologies like nominal sizing alone or using digital corners for analog circuits in new deep-submicron technologies therefore will result in oversized, non-robust and low-yield circuits and products.

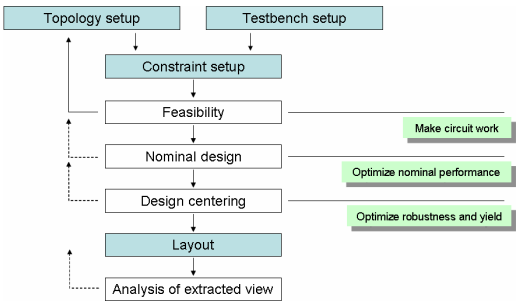


*Figure 3: DFM/DFY Workflow*

Enhanced Design for Yield DFY methodologies follow a three-step approach: Firstly improving the given topology to fulfill all constraints. This ensures that all sizing rules **[15]** are fulfilled and the circuit basically works as it should. To have feasible meaningful circuit solutions is the basic for each performance and yield optimization process. In the second step the circuit will be optimized for nominal circuit performances **[16]** to meet the given specifications. Within this step sensitivities of the circuit performances depending on design parameter changes will be analyzed and the design parameters like widths and lengths of transistors adjusted for optimal values. Correlations will be calculated to reduce dependencies and eliminate further complexities before yield analysis and optimization. In the third step Design Centering the influence of process variations and statistical process parameters will be analyzed for the nominally optimized circuit and a yield optimized solution achieved using a Worst Case Distances **[17]** approach. Local process variations will be analyzed using several Mismatch

Analysis **[18]** methodologies. Industrial applications with reference circuits like operational amplifiers, bandgaps, transimpedance amplifiers a.o. have shown large effects and benefits of a seamless DFM/DFY approach **[19]**.

## 4. Covering the aspects of a seamless industrial designflow integration concept of DFM/DFY *(R. Sommer)*

Circuit designers today have to face a continually improving design complexity but within permanently shorter development time. This process becomes increasingly tedious and time-consuming as more and more performance constraints, design trade-offs, and parasitic effects must be taken into account simultaneously when designing high-performance analog circuits. From technology node to the next technology node increasing parameter variations, especially mismatch effects, (Fig. 2) cause that desired quality targets often cannot be realized within the given time-frame and may even lead to expensive redesigns. One of the reasons is that the number of involved parameters (like BSIM model parameters) and their interdependency with circuit performance becomes so complicated that there is no way to cope with these effects without powerful and intelligent DFM/DFY technology. These tools that e.g. allow calculating a direct yield sensitivity w.r.t. design parameters now enable analog circuit designers to boost quality and speed up the design time. This guarantees to reach the desired design and product requirements already in the first runs and should, supposing that models/parameters are accurate, result in „first time right"-designs. It is clear that such specified functionality can not be obtained for free. Fig. 3 illustrates how more advanced EDA methods relate to more specialized tools, higher complexities for models as well as a need for much more background know how on processes and statistical methods.

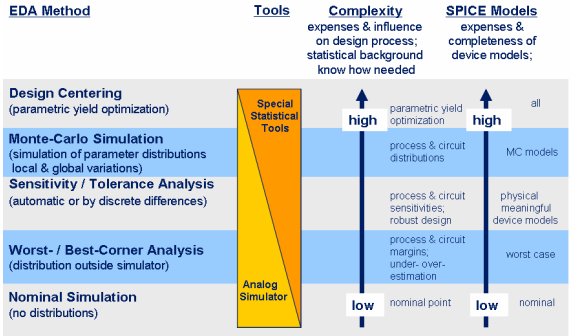


*Figure 3: Circuit Simulation and Yield Optimization Methods*

To cope with today's and tomorrow's design and quality goals, a methodology for a seamless DFM/DFY designflow is required. Up to now, the aforementioned methodology is only available for transistor-level analog simulation, i.e. for circuit blocks up to a few hundred transistors. SSTA – if available – will be an important step in the direction of including higher abstraction levels for the digital parts. On the other hand, a similar methodology is needed for the analog/mixed-signal blocks – an abstraction, how statistical variations can be propagated and incorporated in behavioral models for simulation and optimization on behavioral level and above. Another challenge is to incorporate layout and interconnect effects. Although DFY tools like WiCkeD **[20]** may be used on layout extracted netlists, the computational effort for the simulations becomes extremely high such that the algorithms become infeasible for their application on industrial designs. Hence, the view of a complete top-down and bottom-up design and optimization flow **[21]** is mandatory for leading-edge technologies: Once new methodologies like SSTA, and the analog counterparts for behavioral and layout level are available for industrial requirements they will be adapted and integrated in productive industrial circuit designflows for communication, automotive, memory and other applications **[22]**. To ensure the necessary simulation as well as yield prediction and optimization accuracy between simulated data in front-end design and tested/measured results from manufacturing, a tight link to process characterization and control will be mandatory: The traditional boundary between design and manufacturing will vanish in the future.

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