MunEDA User Group Meeting 2007

Hilton Munich City
Tuesday, September 25th, 2007
1. What’s new

2. Optimization of I/O Macro Cells with WiCkeD

3. Designflow Architecture and Integration of Statistical Sizing Methods in STMicroelectronics Non-Volatile-Memory (NVM) and Automotive Flow

4. Robust and Reliable Analog Design for Automotive and Sensor Applications by Combining Design Centering and SOA Techniques

5. MunEDA Tools and R&D-Roadmap

6. Automatic Analog Circuit Synthesis using WiCkeD

7. Integration of Statistical Sizing Methods in Infineon Analog-Mixed-Signal-Flow

8. Analysis and Optimization of a CMOS Mixer Circuit

9. PLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time

10. Challenges in Analog/Mixed-Signal EDA

11. WiCkeD Circuit Optimization Examples:
   A) Optimization and Centering of the Basic Cells of SRAM Memories
   B) Performance & Yield Optimiz. of Sense Amp for Automotive Applications

12. Qualification of WiCkeD for the austriamicrosystems DFM-DFY design flow


14. Technology Setup for WiCkeD in X-FAB CMOS and BiCMOS Process for Automotive and Sensor Applications

15. Special Topics:
   - IP Porting
   - Local Variations (Analog & Digital)
# List of Participants MunEDA User Group Meeting 2007

<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barth</td>
<td>Michael</td>
<td>Bosch GmbH</td>
</tr>
<tr>
<td>Beck</td>
<td>Kilian</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Böhme</td>
<td>Enno</td>
<td>ZMD AG</td>
</tr>
<tr>
<td>Dr. Boos</td>
<td>Volker</td>
<td>IMMS gGmbH</td>
</tr>
<tr>
<td>Dr. Brockhaus</td>
<td>Martin</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Daglio</td>
<td>Pierluigi</td>
<td>STMicroelectronics</td>
</tr>
<tr>
<td>Fischer</td>
<td>Bernd</td>
<td>National Semiconductor Germany AG</td>
</tr>
<tr>
<td>Fischer</td>
<td>Horst</td>
<td>Qimonda AG</td>
</tr>
<tr>
<td>Frevert</td>
<td>Ronny</td>
<td>Fraunhofer IIS</td>
</tr>
<tr>
<td>Georgakos</td>
<td>Georg</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Glöckel</td>
<td>Volker</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Dr. Gondro</td>
<td>Elmar</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Gräb</td>
<td>Helmut</td>
<td>TU München</td>
</tr>
<tr>
<td>Grasenack</td>
<td>Ben</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Hebenstreit</td>
<td>Andreas</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Hennig</td>
<td>Eckhard</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Knöchel</td>
<td>Uwe</td>
<td>Fraunhofer IIS</td>
</tr>
<tr>
<td>Kraußé</td>
<td>Dominik</td>
<td>TU Ilmenau</td>
</tr>
<tr>
<td>Lengfeldner</td>
<td>Roland</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Lukashevich</td>
<td>Dzianis</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Mauthe</td>
<td>Manfred</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Mörth</td>
<td>Thomas</td>
<td>austriamicrossystems AG</td>
</tr>
<tr>
<td>Müller</td>
<td>Daniel</td>
<td>TU München</td>
</tr>
<tr>
<td>Neubauer</td>
<td>Harald</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Dr. Obermeier</td>
<td>Bernd</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Pieper</td>
<td>Klaus-Willi</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Pronath</td>
<td>Michael</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Qin</td>
<td>Zikai</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Qiu</td>
<td>Jin</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Raciti</td>
<td>Elena</td>
<td>STMicroelectronics</td>
</tr>
<tr>
<td>Ripp</td>
<td>Andreas</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Rooch</td>
<td>Karl-Heinz</td>
<td>ZMD AG</td>
</tr>
<tr>
<td>Dr. Rotter</td>
<td>Peter</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Sattler</td>
<td>Sebastian</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Schenkel</td>
<td>Frank</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Dr. Schrader</td>
<td>Lothar</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Dr. Sobe</td>
<td>Udo</td>
<td>ZMD AG</td>
</tr>
<tr>
<td>Dr. Prof. Sommer</td>
<td>Ralf</td>
<td>IMMS gGmbH</td>
</tr>
<tr>
<td>Dr. Sporrer</td>
<td>Christian</td>
<td>Infineon AG</td>
</tr>
<tr>
<td>Sylvester</td>
<td>Matthias</td>
<td>MunEDA GmbH</td>
</tr>
<tr>
<td>Trautner</td>
<td>Uwe</td>
<td>Synopsys Inc.</td>
</tr>
<tr>
<td>Wang</td>
<td>Xiaoying</td>
<td>Universität Frankfurt</td>
</tr>
</tbody>
</table>
Dear MunEDA User,

We cordially invite you to come to our MunEDA User Group Meeting 2007 - MUGM07 - in Munich. Goal of the event is the intensive exchange of experience by industrial users of MunEDA’s DFM-DFY software tools. We are very pleased to gain excellent speakers and contributions for this MunEDA User Group Meeting. Besides other contributions one main focus of the MunEDA User Group Meeting 2007 is the special topic:

Design Flow & Technology Integration of Nominal and Statistical Sizing Methods

Date: September 25-26th 2007
Location: Hilton Munich City
Rosenheimer Straße 15
81667 Munich - Germany

MunEDA User Group Meeting 2007 Agenda will contain contributions from:

- Infineon
- STMicroelectronics
- Qimonda
- Infineon
- austriamicrosystems
- TUM
- Synopsys
- IMES
- FAB

and others …

Presentation Topics of MUGM2007:

- Integration of Statistical Sizing Methods in Analog-Mixed-Signal-Flow
- Automatic Analog Circuit Synthesis using WiCkeD
- Robust and Reliable Analog Design for Automotive and Sensor Applications
- Memory - PLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time
- Technology setup for WiCkeD in CMOS and BiCMOS Process for Automotive and Sensor Applications
- Optimization of I/O Macro Cells with WiCkeD
- Introduction of Analog IP Porting Flow Concept
- Automatic Flow for Library Cell Optimization
- Basics of Analog Circuit Modelling and Simulation
- Analysis and Optimization of a CMOS Mixer Circuit
- And more…

We are very looking forward to welcome you to our MunEDA User Group Meeting 2007 in Munich.

Andreas Ripp
Vice President Sales & Marketing

AND YOUR TEAM

Dr. Michael Pronath
Vice President Products & Solutions

Participation for MUGM07 is free but early registration and accommodation is highly recommended because of co-located Munich Oktoberfest.
<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>09.30 h - 10.00 h</td>
<td>Registration &amp; Welcome Coffee</td>
<td></td>
</tr>
<tr>
<td>10.00 h - 10.30 h</td>
<td>Welcome &amp; Whats new</td>
<td>Andreas Ripp, VP Sales &amp; Marketing, MunEDA GmbH</td>
</tr>
<tr>
<td>10.30 h - 11.00 h</td>
<td>Optimization of I/O Macro Cells with WiCkeD</td>
<td>M. Mauth, Senior Staff Engineer, Infineon AG / A. Hebenstreit, Staff Engineer, Infineon AG</td>
</tr>
<tr>
<td>11.00 h - 11.20 h</td>
<td>Coffee &amp; Discussion Break</td>
<td></td>
</tr>
<tr>
<td>11.20 h - 11.50 h</td>
<td>Designflow Architecture and Integration of Statistical Sizing Methods in STMicroelectronics Non-Volatile-Memory (NVM) and Automotive Flow</td>
<td>P. Daglio, NVM Mixed-Signal Design Flow Program Manager, STMicroelectronics</td>
</tr>
<tr>
<td>11.50 h - 12.20 h</td>
<td>Robust and Reliable Analog Design for Automotive and Sensor Applications by Combining Design Centering and SOA Techniques</td>
<td>U. Sobe, ZMD AG / K.-H. Roock, ZMD AG</td>
</tr>
<tr>
<td>12.20 h - 13.30 h</td>
<td>Lunch Break</td>
<td></td>
</tr>
<tr>
<td>13.00 h - 13.45 h</td>
<td>HOT-Topics</td>
<td>J. Qiu, MunEDA GmbH</td>
</tr>
<tr>
<td>13.45 h - 14.15 h</td>
<td>MunEDA Tools and R&amp;D-Roadmap</td>
<td>F. Schenkel, VP Research &amp; Development, MunEDA GmbH</td>
</tr>
<tr>
<td>14.15 h - 14.45 h</td>
<td>Automatic Analog Circuit Synthesis using WiCkeD</td>
<td>X. Wang, Johann-Wolfgang Goethe Universität Frankfurt am Main</td>
</tr>
<tr>
<td>14.45 h - 15.00 h</td>
<td>Coffee &amp; Discussion Break</td>
<td></td>
</tr>
<tr>
<td>15.00 h - 15.20 h</td>
<td>Integration of Statistical Sizing Methods in Infineon Analog-Mixed-Signal-Flow</td>
<td>E. Hennig, CAD Staff Engineer, Infineon AG</td>
</tr>
<tr>
<td>From 15.45 h</td>
<td>Social Event: Transfer to MunEDA Event at Munich Oktoberfest</td>
<td></td>
</tr>
</tbody>
</table>

**Day 2 – Wednesday, September 26th, 2007**

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>09.00 h - 10.00 h</td>
<td>Speakers Breakfast</td>
<td></td>
</tr>
<tr>
<td>10.00 h - 10.30 h</td>
<td>PLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time</td>
<td>J. Zou, Qimonda AG / H. Gräb, D. Müller and U. Schlichtmann, Technische Universität München</td>
</tr>
<tr>
<td>10.30 h - 11.15 h</td>
<td>Preliminary Title: Basics of Analog Circuit Modelling and Simulation</td>
<td>R. Sommer, TU Ilmenau / IMMS gGmbH</td>
</tr>
<tr>
<td>11.15 h - 11.30 h</td>
<td>Coffee &amp; Discussion Break</td>
<td></td>
</tr>
<tr>
<td>11.30 h - 12.00 h</td>
<td>WiCkeD Circuit Optimization Examples:</td>
<td></td>
</tr>
<tr>
<td>A) Optimization and Centering of the Basic Cells of SRAM Memories</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B) Performance and Yield Optimization of Sense Amplifier for Automotive Applications</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12.00 h - 12.30 h</td>
<td>Qualification of WiCkeD for the austriamicrosystems DFM-DFY design flow</td>
<td>T. Möhr, Section Manager Design Support, austriamicrosystems AG</td>
</tr>
<tr>
<td>12.30 h - 13.30 h</td>
<td>Lunch Break</td>
<td></td>
</tr>
<tr>
<td>13.30 h - 14.00 h</td>
<td>Automatic Flow for Library Cell Optimization</td>
<td>K. Singhal, Synopsys Inc. / T. Vogels, Senior Applications Engineer, MunEDA Inc.</td>
</tr>
<tr>
<td>14.00 h - 14.30 h</td>
<td>Technology Setup for WiCkeD in X-FAB CMOS and BiCMOS Process for Automotive and Sensor Applications</td>
<td>V. Boos, IMMS gGmbH / H. Wald, X-Fab Semiconductor Foundries AG</td>
</tr>
<tr>
<td>14.30 h - 15.00 h</td>
<td>Coffee &amp; Discussion Break</td>
<td></td>
</tr>
<tr>
<td>15.00 h - 15.45 h</td>
<td>Special Topics:</td>
<td></td>
</tr>
<tr>
<td>- IP Porting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Local Variations (Analog &amp; Digital)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15.45 h - 16.00 h</td>
<td>Wrap-up Discussion and End of Conference</td>
<td>Andreas Ripp, VP Sales &amp; Marketing, MunEDA GmbH</td>
</tr>
<tr>
<td>16.00 h - 16.30 h</td>
<td>Farewell Coffee &amp; Discussion</td>
<td></td>
</tr>
</tbody>
</table>
Optimization of I/O Macro Cells with WiCkeD

Manfred Mauthe  
Senior Staff Engineer  
manfred.mauthe@infineon.com

Andreas Hebenstreit  
Staff Engineer  
andreas.hebenstreit@infineon.com

Infineon AG  
www.infineon.com

About Infineon
Infineon Technologies AG, Munich, Germany, offers semiconductor and system solutions for applications in the wired and wireless communications markets, for security systems and smartcards, for the automotive and industrial sectors, as well as memory products. With a global presence, Infineon operates in the US from San Jose, CA, in the Asia-Pacific region from Singapore and in Japan from Tokyo, with about 33,800 employees worldwide. In the mobile radio area, Infineon Technologies is one of the leading suppliers of integrated circuits. Infineon has been participating in a variety of funding projects concerning EDA, so recently in SpeAC, ANASTASIA, MESDIE, ASDESE, LoMoSA, VISION, RapidMPSoC. Due to newest CMOS technology highly integrated solutions for cellular communication systems, local area systems, high performance data communication, and satellite navigational systems can be provided.
Optimization of I/O Macro Cells with WiCkeD

Manfred Mauthe
Andreas Hebenstreit
COM BTS LIB IO

Table of contents

- Introduction
- I/O Macro Cells
- Example 1: LVDS Driver
- Example 2: Pre-amplifier
- Example 3: USB Charger Detector
- Conclusion
Table of contents

- Introduction
- I/O Macro Cells
- Example 1: LVDS Driver
- Example 2: Pre-amplifier
- Example 3: USB Charger Detector
- Conclusion

I/O Macro Cells

- I/Os enable off-chip data transfer
- In contrary to standard I/O cells I/O macro cells are more complex.
- Macro cells may include: Transmitter, receiver, impedance control circuit, serializer, deserializer, CDR, levelshifter, bandgap reference, current and bias voltage sources, V/I converter, OPA, voltage regulator, voltage level detector, short/overload detector ...
Components of an I/O Macro Cell

An I/O macro cell includes at least one transmitter or receiver block.
Examples of I/O Macros

- LVDS transmitter and receiver
- USB, USB1.1, USB2.0, USB OTG
- DDR1, DDR2, DDR3 transceiver
- PCIe transceiver

Typical Circuit Characteristics

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>High/low levels, rise/fall time, delay, duty cycle, jitter</td>
</tr>
<tr>
<td></td>
<td>Differential: cross over, common mode</td>
</tr>
<tr>
<td>Diff. Receiver</td>
<td>Sensitivity, delay, duty cycle, jitter</td>
</tr>
<tr>
<td>Schmitt Trigger</td>
<td>Switching threshold, delay, duty cycle</td>
</tr>
<tr>
<td>Biasing</td>
<td>Vref accuracy, Iref accuracy, PSSR</td>
</tr>
<tr>
<td>Level Shifter</td>
<td>Delay, rise/fall time, cross over, shift margin</td>
</tr>
<tr>
<td>Voltage Regulator</td>
<td>Stability, accuracy, dynamic behaviour</td>
</tr>
<tr>
<td>Opamp</td>
<td>DC-gain, phase margin ...</td>
</tr>
<tr>
<td>Single-ended, differential output</td>
<td></td>
</tr>
</tbody>
</table>
Table of contents

- Introduction
- I/O Macro Cells
- Example 1: LVDS Driver
- Example 2: Pre-amplifier
- Example 3: USB Charger Detector
- Conclusion

Example 1: LVDS Transmitter Macro Cell

![Diagram of LVDS Transmitter Macro Cell]

- Data_IN
- Single-ended to differential
- Pre-amplifier
- Driver
- Bandgap
- Voltage Converter
- ESD
- To PAD
- R=100Ω
LVDS Driver Schematic

Replica

Driver stage

LVDS Output Impedance

Simulation of switch impedance

Expansions: Resistance of LVDS switches

red  T=150°C
green T= 27°C
blue T= -40°C
Simulation Setup for LVDS Driver

Testbench: DC and TRN

Driver Output Impedance

<table>
<thead>
<tr>
<th>$R_{out}$</th>
<th>$V_{ohi-Voalo}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>140 $\Omega$</td>
<td>295 mV</td>
</tr>
<tr>
<td>40 $\Omega$</td>
<td>178 mV</td>
</tr>
</tbody>
</table>

Optimization Results

Optimized Output Impedance

<table>
<thead>
<tr>
<th></th>
<th>nom</th>
<th>slow</th>
<th>fast</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{oa}$ [$\Omega$]</td>
<td>65</td>
<td>138</td>
<td>41</td>
</tr>
<tr>
<td>$R_{ob}$ [$\Omega$]</td>
<td>64</td>
<td>128</td>
<td>41</td>
</tr>
</tbody>
</table>
Example 2: Pre-Amplifier in USB20 PHY
The pre-amplifier has also the function of a level shifter.
Setting Expressions

- DEL_DP2_DN2_short01
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 1 "rising"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 1 "rising"

- DEL_DP2_DN2_long10
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 2 "falling"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 2 "falling"

- DEL_DP2_DN2_short10
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 3 "falling"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 3 "falling"

- DEL_DP2_DN2_long01
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 3 "falling"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 3 "falling"

- jitterDP2_01 = diff(long01-short01
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 3 "falling"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 3 "falling"

- jitterDP2_10 = diff(long10-short10
  - delay(clip((VT("/DP1")-VT("/DN1")) 1e-09 3e-08) 0 2 "falling"
  - clip((VT("/DP2")-VT("/DN2")) 1e-09 3e-08) 0 2 "falling"

Optimization Results
Eye Diagrams for process corners

Reduction of overall jitter by 10% from 120ps to 107ps

Table of contents

- Introduction
- I/O Macro Cells
- Example 1: LVDS Driver
- Example 2: Pre-amplifier
- Example 3: USB Charger Detector
- Conclusion
Charger Detector ("Battery Charging Specification 1.0")

Vtest = 600 mV ± 17% = 500 mV … 700 mV @ I(D+) = 0 μA … 200 μA
Vdat_ref = 325 mV ± 23% = 250 mV … 400 mV

Large tolerances but limiting design constraints:
- Simple circuit
- No external current or voltage reference
- Use 1.2V ± 5% supply instead
- OV/UV at D+/D- pins
- ESD demands
- No high voltage devices

Design not so straight forward

Circuit concept, sources of error, testbench

Orange: Generated from 1.2V ± 5% supply using poly resistors
Green: Performances to be measured
Purple: Test signals
Transistor level implementation (simplified)

- Design parameters for overall optimization
- Voltage regulator and voltage comparator blocks optimized in separate setups
- Additional performances: Currents in voltage dividers, currents mirrored to voltage regulator and comparator

Optimization flow and results

- Start → DetOpt (least square initial)
- → DetOpt (parm. Distance initial)
- → DetOpt (parm. Distance at worst case values)
- → YieldOpt

This Monte Carlo analysis was performed with operating parameters set to initial, worst-case, and corner values.
From experience (I)

- Do not blindly go into optimization with randomly selected design parameters and just accept results.

- Break down into independent blocks, optimize separately.

- Find out the set of design parameters (W, L, R, C, ...) critical to the design. Restrict optimization to these.

- Less design parameters enable at least qualitative understanding (plausibility) of what is going on (why is the optimizer going in that direction ... ?).

- Less design parameters reduce computing time.
From experience (II)

- Strange optimization results may hint to conceptual weakness in a circuit.
- WiCkeD provides very good overview of results during work in progress.
- Some pragmatic hints in the WiCkeD online documentation on choosing available options (e.g. algorithms, check buttons like “always calculate at worst case values”, ...) would be useful. What is practically the difference? What are pros and cons?

Conclusion

- Handling of WiCkeD is easy (integrated in Design Flow, stable).
- Understanding WiCkeD and its features comes with using it.
- We find that WiCkeD improves confidence in results of design work.
- We find that WiCkeD allows for better quality in I/O Macro circuit design. Notably by circuit verification in a complete and documented way.
- We always received very good and fast support from MunEDA.
THANK YOU FOR YOUR ATTENTION!
Designflow Architecture and Integration of Statistical Sizing Methods in STMicroelectronics Non-Volatile-Memory and Automotive Flow

Pierluigi Daglio
AMS Flows & Methods Manager NVM Design Platform, FTM Central CAD & Design Solutions
pierluigi.daglio@st.com

STMicroelectronics
www.st.com

About STMicroelectronics
STMicroelectronics is one of the world’s largest semiconductor companies with net revenues of US$9.85 billion in 2006 and US$4.69 billion for the first half of 2007.

The Company’s sales are well balanced between the semiconductor industry’s five major high-growth sectors (percentage of ST’s sales in 2007): Communications (35%), Consumer (17%), Computer (16%), Automotive (16%) and Industrial (16%).

According to the latest industry data, ST is the world’s fifth largest semiconductor company with market leadership in many fields. For example, ST is the leading producer of application-specific analog chips and power conversion devices. It is also the #1 supplier of semiconductors for the Industrial market and for set-top box applications, and occupies leading positions in fields as varied as discrete devices, camera modules for mobile phones and automotive integrated circuits.
Design Flow Architecture and Statistical Sizing Methods Integration in STMicroelectronics Non Volatile Memory and Automotive Flows

Pierluigi Daglio
NVM AMS Flows & Methods Manager
Non Volatile Memories Design Platform
Central CAD & Design Solutions
Key Topics in Deep Submicron

- Several applications are moving from fully digital to mixed-signal domain integrating sensitive analog parts and often embedding flash memories.

- Full chip PLS with parasitic components and IR drop analysis are everyday more tricky whereas at the same time become strictly mandatory before going to fabrication.

- Very deep submicron technologies with wide process variations (variability) require nominal optimization and statistical design analysis processes both at cell level and block/IP level to enhance and optimize yield.

- A really robust and efficient AMS design flow including AMS verification is mandatory to go to fabrication with the minimum risk of failure.

- Usage of circuit/spice checks and Safe Operating Area (SOA) capabilities will dramatically increase and become sign-off for all design teams.
Designer Today Dilemmas

- Speed or accuracy?
- Analog circuit optimization by hand or automated tool?
- Yield optimization? How good are statistical models?
- Real AMS environment or fast spice simulation?
- Analog signal visual checks or automated checks?
- AMS code coverage?
- Investing resources to learn new tools?
AMS Full Design Flow for NVM/APG

WiCkeD Design & Optimization Flow

- Eldo netlist
- Technology

**INPUT FILES**

**Circuit setup**

**Circuit analysis**

**Circuit optimization**

**Final analysis**

**WiCkeD ENVIRONMENT**

**OPTIMIZATION STEPS**
1. Feasibility optimization
2. Nominal optimization
3. Yield optimization

❖ User controlled step-by-step optimization process
❖ Designers check changes after each optimization step and decide whether to go on or alter some settings
WiCkeD Design & Optimization Flow

Circuit Analysis

Change Circuit Settings
→ Simulation
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Nominal Optimization

Nominal Optimization
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Feasibility Optimization

Yield Optimization
→ Worst-Case Analysis
→ MCA

Wiscon Design & Optimization Flow

Circuit Analysis

Change Circuit Settings
→ Simulation
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Nominal Optimization

Nominal Optimization
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Feasibility Optimization

Yield Optimization
→ Worst-Case Analysis
→ MCA

Wiscon Design & Optimization Flow

Circuit Analysis

Change Circuit Settings
→ Simulation
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Nominal Optimization

Nominal Optimization
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Feasibility Optimization

Yield Optimization
→ Worst-Case Analysis
→ MCA

Wiscon Design & Optimization Flow

Circuit Analysis

Change Circuit Settings
→ Simulation
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Nominal Optimization

Nominal Optimization
→ Sensitivity Analysis
→ Worst-Case Operation
→ Structural Constraints fulfilled?
→ Feasibility Optimization
→ Structural Constraints fulfilled?
→ MCA

Feasibility Optimization

Yield Optimization
→ Worst-Case Analysis
→ MCA
WiCkeD Integration into ST Design Framework

- WiCkeD is fully integrated into ST Unicad 2.4 design framework
  - Internally developed software based on Cadence opus to provide a unified design environment for analog and mixed-signal applications
- WiCkeD is well integrated into ADE (Analog Design Environment)
  - Direct management of all the information related to technology data, model cards, design variables, simulation set up and output results

Two different methodologies can be followed to use the tool
1. If a schematic is available → WiCkeD can be launched from the ADE
2. If only a netlist (*.cir file) is available → WiCkeD can be launched in stand alone mode

WiCkeD Integration into ADE

- Circuit setup into the Unicad ADE environment
  - Automatic inclusion of statistical libraries for all the devices
  - Definition of the input stimuli
  - Definition of the simulation analysis
  - Definition of the circuit performances
  - In Eldo syntax
    - .extract statements
  - In Ocean script syntax
    - Measurement information is extracted directly from ADE
    - Not visible if WiCkeD is launched in stand alone mode with a new netlist
  - Definition of the parameter settings
WiCkeD Integration into ADE

- WiCkeD Constraint Editor can be launched from a menu

<table>
<thead>
<tr>
<th>Design Variables</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Value</td>
</tr>
<tr>
<td>e</td>
<td>4n</td>
</tr>
<tr>
<td>e</td>
<td>800n</td>
</tr>
<tr>
<td>e</td>
<td>4u</td>
</tr>
<tr>
<td>e</td>
<td>10u</td>
</tr>
<tr>
<td>e</td>
<td>10u</td>
</tr>
</tbody>
</table>

Schematic Window

WiCkeD Design Flow Overview

Analog Design Environment

Waveform Window

WiCkeD Results
Examples of Particular WiCkeD Usage

- **Modeling** group verifies the quality of the statistical model cards
  - Perform circuit analysis (sensitivity and MCA)
  - Compare statistical models based on PCA (Principal Component Analysis) with respect to statistical models based on real process parameters
  - Check model accuracy and links between different representations

- **Examples of Particular WiCkeD Usage**
  - **Modeling** group analyses the impact of different kinds of statistical models on circuit performances
  - Comparison between **SNM_r** (Static Noise Margin in read mode) obtained with two Montecarlo analyses based respectively on Crolles and Multifab statistical models

  - The mean value is the same for the two histograms but the standard deviation is larger when using stat_multifab data
Examples of Classic WiCkeD Usage

Examples of classic usage of the flow for real applications:

- **FTM** group improved the leakage current of a SRAM core (4096 basic cells in CMOS 90nm) keeping, at the same time, good values for all the other performances.

- **Automotive** group analysed in which conditions a critical sense amplifier did not work and enhanced its robustness to the variations of both process and operating parameters.

- **Flash Memory** group improved the delay of a specific signal through a safety timer in a 1Gb flash memory to guarantee a safe and correct working.

Some WiCkeD Projects in STM in 2007

<table>
<thead>
<tr>
<th>Topology</th>
<th>Technology</th>
<th>Target</th>
<th>Analysis</th>
<th>Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Cell – SRAM</td>
<td>CMOSM10</td>
<td>Leakage optimization</td>
<td>Circuit analysis &amp; design centering</td>
<td>FTM Agrate</td>
</tr>
<tr>
<td>Core (4096 cells)</td>
<td>HCMOS9</td>
<td>Leakage optimization</td>
<td>Circuit analysis &amp; design centering</td>
<td>FTM Agrate</td>
</tr>
<tr>
<td>SRAM - SP10LLC</td>
<td>CMOSM10</td>
<td>Leakage optimization</td>
<td>Circuit analysis &amp; design centering</td>
<td>FTM Agrate</td>
</tr>
<tr>
<td>Core (512 cells)</td>
<td>CMOST11</td>
<td>Delay time optimization</td>
<td>Circuit analysis &amp; design centering</td>
<td>FMG Agrate</td>
</tr>
<tr>
<td>SRAM - CMOST11</td>
<td>(65nm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandgap</td>
<td>HCMOS8S</td>
<td>Worst case analysis</td>
<td>Circuit analysis</td>
<td>APG Castelletto</td>
</tr>
<tr>
<td></td>
<td>(180nm)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Some WiCkeD Projects in STM in 2007

<table>
<thead>
<tr>
<th>Topology</th>
<th>Technology</th>
<th>Target</th>
<th>Analysis</th>
<th>Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTA DC-DC converter</td>
<td>CMOS065 (65nm)</td>
<td>Yield improvement</td>
<td>Circuit analysis &amp; design centering</td>
<td>MMC Grenoble</td>
</tr>
<tr>
<td>Single transistor</td>
<td>CMOST11, CMOSM10</td>
<td>Comparison between different statistical models</td>
<td>Circuit analysis</td>
<td>MPG Agrate, FMG Agrate</td>
</tr>
<tr>
<td>Single transistor &amp; SRAM core</td>
<td>CMOSM10, CMOSF9 (130nm)</td>
<td>Comparison between different statistical models</td>
<td>Circuit analysis</td>
<td>MPG Agrate, FTM Agrate</td>
</tr>
<tr>
<td>Core (4096 cells) SRAM</td>
<td>CMOSM10</td>
<td>Leakage optimization</td>
<td>Circuit analysis &amp; design centering</td>
<td>FTM Agrate</td>
</tr>
<tr>
<td>Sense amplifier</td>
<td>CMOSM10</td>
<td>Worst case analysis &amp; yield improvement</td>
<td>Circuit analysis &amp; design centering</td>
<td>APG Agrate</td>
</tr>
</tbody>
</table>

These two examples will be presented in details tomorrow at 11:30

Design Manager Commitment

- WiCkeD is a perfect tool for circuit analysis, design optimization and yield enhancement
- Often design managers do not want designers to lose time to learn new tools
- Often design managers ask for design services instead of support and methodology deployment to their designers
- Directors should push design managers to use new tools for sign-off before sending the project to the fabrication
Conclusions

- Several benchmarks and real applications with WiCkeD in STM proved it helps to design more robust circuits with a better yield.
- Design managers should push designers to apply new methodologies as mandatory sign-off before sending the project to the fabrication.
- Lack of design manager commitment leads to a gap between current design methodology and CAD advanced solutions.
- Need to align the management chain between CAD and divisions.

THANK YOU !!!

AMS Design Flows & Methods
Robust and Reliable Analog Design for Automotive and Sensor Applications by Combining Design Centering and SOA Techniques

About ZMD
ZMD was founded in 1961 and over the past 45 years it has played a significant role in the rapid development of the microelectronics industry to becoming one of the most innovative key industries of the 21st century. The company is said to be the cradle of the Saxon microelectronics industry and is a founder of the largest European semiconductors cluster, “Silicon Saxony”. Since privatisation in 1999, ZMD has maintained its path of success. During this period of time, ZMD has invested around €120 million in equipment and buildings as well as €100 million in product development.
Robust and Reliable Analog Design
for Automotive and Sensor Applications
by Combining Design Centering and SOA Techniques

Udo Sobe, Karl-Heinz Rooch and Michael Pronath

Outline

• Motivation
• Design Centering
• Constraints matrix
• Examples
• Summary
Motivation

- ICs for automotive application need a combination of
  - Robustness (DFY)
  - Reliability (DFR)

- Design centering techniques are state of the art for yield improvement

- Reliability parameters for reliability simulation are not standard in the process design kits (PDK)

- Current PDK provide information about limits:
  - Maximum voltage difference
  - Maximum current density
  - Safe operating area (SOA)

- Limits have to be available within the
  - Design environment (Cadence: ADE/Device Checking)
  - Verification tool (ZMD in-house: zmdAnalyser) and
  - Optimization tool (MunEDA: WiCkE D)

Design Centering - Sensitivity

Observation: Statistical and reliability models use the same model parameter to describe variation and degradation respectively.

Idea: If we reduce sensitivity to such model parameters then our circuit should be less affected by both process variation and degradation.

Conclusion: Robust and reliable circuit design requires analysis and optimization of sensitivity to parameter shift.
The worst-case point is the parameter set of highest probability density for which a parametric fault occurs.

Design Centering - Effect of Process Drift or Degradation on Yield

Thought experiment

Yield after production Yield during life time
SOA diagrams define the operating limits of devices
- Several effects are considered
- SOA diagrams are available for special devices in PDKs (e.g. DMOS)
- Different areas mark reliability/stress ranges
  - Operating Area 2: life time (DC) 100h -> parameter degradation <10%
- SOA diagrams are part of design practice

SOA Checking Possibilities

Capsulation of the device models by checker scripts
- Checker is parallel connected to the device
- Script use e.g. verilogA
- Results are submitted into a log file
- Implementation separate or in model library

Device checking from Analog Design Environment (ADE)
- Based on Spectre Assertion
- Violation display shows results
- GUI available since ic5141.usr5
A circuit specification describes only the input-output behavior of a circuit.

Additional constraints on geometrical and electrical properties must be introduced to create functional and robust designs.

Constraints correspond to the used basic design structures in the circuit.

WiCkeD supports a constraints matrix for a lot of basic design structures, e.g. current mirrors, differential input pairs, ...

They can be generated semi-automatically by structure recognition, with manual adaption by the designer.

How can we combine the conventional SOA method with constraint matrix?

Constraints matrix is extended to reflect reliability aspect of SOA diagrams.

Function, robustness and reliability criteria can be considered together for verification/optimization by the constraints matrix.
Fully differential OTA in ZMDs 0.6μm CMOS technology with self regulated cascodes for automotive applications

Task: development of a new topology

Operating:
- temp: -40 … 150°C
- vsupp: 4.5 … 5.5 V
- cl0ad: 3 …… 9 pF

Design parameters: 70 (sequentially used)

Devices: ca. 130

Proceeding:
- feasibility optimization
- design centering
- worst case distance analysis
- iterative improvement of the topology
- stability analysis by SPECTRE
- reducing device stress by SOA constraints

### Design Centering Results – OTA (I)

<table>
<thead>
<tr>
<th>parameter</th>
<th>goal</th>
<th>yield [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC_Gain</td>
<td>&gt;110 dB</td>
<td>99</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>&gt;50 Mhz</td>
<td>100</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>50 ° ... 80 °</td>
<td>99</td>
</tr>
<tr>
<td>Setting Time 0.01%</td>
<td>&lt; 100 ns</td>
<td>100</td>
</tr>
<tr>
<td>Offset</td>
<td>± 10 mV</td>
<td>100</td>
</tr>
<tr>
<td>i_supp</td>
<td>&lt; 2.5 mA</td>
<td>100</td>
</tr>
<tr>
<td>PM_CMFB</td>
<td>25 ° ... 80 °</td>
<td>100</td>
</tr>
</tbody>
</table>

- Self biasing cascode (SBC) are applied for high DC gain > 110dB
- High currents are possible, particularly in the output stage

### Design Centering Results – OTA (II)

- Stress of the most critical part M1 can be limited by defining the drain-source voltage $v_{ds}$ of M1 just above the saturation voltage $v_{dsat}$

<table>
<thead>
<tr>
<th>geometrical</th>
<th>electrical</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{1}=L_{2}$</td>
<td>$v_{c1}-v_{ch} &gt; v_{dsat}$</td>
</tr>
<tr>
<td>$v_{ch}-v_{in}$</td>
<td>$v_{ds}=v_{ch}=v_{in}$</td>
</tr>
<tr>
<td>$v_{ds1} &lt; v_{ds2}$</td>
<td>$v_{ds1} &lt; \text{effmax}$</td>
</tr>
</tbody>
</table>

- $L > \lambda_{min}$
- $W > \lambda_{max}$
- $L \times W > \lambda_{max}$

reliability

\[ V_{ds1} - |V_{gs1} - V_{th1}| < V_{dsat,max} \]
Design Centering Results – OTA (III)

• Chip photo of the realized OTA with final count of 95 transistors, 20 capacitors and 9 resistors

Design Centering Results – LIN transceiver (I)

Local Interconnect Network (LIN) transceiver for automotive communication system

Task: minimize deviation (centering) of the key parameter, symmetry of transmitter propagation delay, to ±2us

Operating: temp: -40 ... 140°C
vsupp: 6.5 ... 18 V

Design parameters: 27

Devices: ca. 300

Proceeding:
- Monte Carlo analysis
- parameter screening
- feasibility optimization
- design centering
- SOA constraints for the output driver stage

<table>
<thead>
<tr>
<th>Performance</th>
<th>Design</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>initial</td>
<td>centered A</td>
</tr>
<tr>
<td>Yield</td>
<td>71%</td>
<td>95%</td>
</tr>
<tr>
<td>Worst Case Distance</td>
<td>0.56σ</td>
<td>1.64σ</td>
</tr>
<tr>
<td>Additional Area</td>
<td>-</td>
<td>80x80um²</td>
</tr>
</tbody>
</table>
Design Centering Results – LIN transceiver (II)

Design centered B: IREF

Design centered A: Slew Rate Control

Design Centering Results – LIN transceiver (III)

- Constraints matrix for high voltage devices
- Checking via constraint matrix of the high voltage devices in the marked stages

<table>
<thead>
<tr>
<th>Function</th>
<th>geometrical</th>
<th>electrical</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_{GS} - V_{TH} &gt; V_{MIN}$ $V_{DS} - (V_{F3} - V_{TH}) &gt; V_{MIN}$</td>
</tr>
<tr>
<td>robustness</td>
<td>$L &gt; L_{MIN}$ $W &gt; W_{MIN}$</td>
<td>$I_{DSS} &gt; I_{DSS_{MIN}}$</td>
</tr>
<tr>
<td>reliability</td>
<td>$V_{DS} &lt; V_{DS_{MAX}}$</td>
<td>$V_{GS} &lt; V_{GS_{MAX}}$</td>
</tr>
</tbody>
</table>
Comparison of SOA Checking

<table>
<thead>
<tr>
<th>Basis</th>
<th>Model Capsulation</th>
<th>ADE Device Checking</th>
<th>Constraint Matrix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single device</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Device type</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Results Format</td>
<td>Log file</td>
<td>Violation display</td>
<td>Constraint parameter</td>
</tr>
<tr>
<td>Verification</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Optimization</td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

Summary

- Design centering techniques are appropriate to reduce sensitivity of circuit performance wrt. changes of device parameters.
- A systematic constraints matrix which covers function, robustness and reliability criteria can be defined for basic design structures.
- SOA methodology is available in the PDKs and can be used for reliability definitions in the constraint matrix.
- Combination of design centering and consideration of SOA constraints is one key to designing robust and reliable circuits.
- Outlook: our future intention will be focused on life-time problems and once again on substrate current.
MunEDA Tools and R&D-Roadmap

Dr. Frank Schenkel
Vice President Research & Development
frank.schenkel@muneda.com

MunEDA GmbH
www.muneda.com

About MunEDA
MunEDA provides leading EDA technology for analysis and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA's products and consulting enable customers to reduce the design times of their circuits and to maximize robustness and yield. MunEDA's solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

WiCkeD is a comprehensive and powerful software productive for interactive, manual, semi- and fully automatic analysis, sizing, design centering and yield optimization of analog and mixed-signal circuits. WiCkeD is marketed also under the trademark DesignMD®.

MunEDA was founded in 2001 and is a privately held company. The company headquarter is located in Munich, Germany.

MunEDA's sales & support channel in North America is MunEDA Inc. headquartered in Sunnyvale, CA, USA. Distributor in Taiwan is GTI Inc. (www.grandti.com.tw) and in Korea DAOU Xilicon (www.daouxilicon.com).
MunEDA Tools and R&D Roadmap

Dr. Frank Schenkel
VP Research & Development, MunEDA GmbH

LEGAL NOTICE
Information contained in this presentation reflects MunEDA’s plans as of the date of this presentation. Such plans are subject to completion and subject to change. Products may be offered and purchased only pursuant to an authorized quote and purchase order.
New in Version 5.2

Overview

• Detailed log-files for all optimizers
• Re-organized result display in worst-case operation node
• Confidence intervals for parameter influences (Monte Carlo)
• New option to check all operating corners
• Better load balancing for simulation servers
• Support parsing netlists of large designs (>1000 devices)
Overview (2)

- Auto synchronization of simulation data & design history
- Improved scrolling of tables
- Functionality to call application in simulation sub-directory
- Bugfixes
- Supported operating systems

Log-Files

- Problems that occur during an optimization can be identified more easily, e.g., which constraints prevent further optimization.
- It can be seen whether simulation errors occurred during the optimization/analysis.
- If the current circuit project is confidential, designers can still send the log-file to our support team.
Log-Files (2)

- Verbosity for logging can be set/changed
  - At startup (via command line)
  - During runtime
  - For every component individually
  - For all components together

Result Display in Worst-Case Operation

- Better comparison of lower and upper worst-cases
- Added display of nominal performance values
- Added display of specification values per performance (if available, “min”, “max” otherwise)
Monte Carlo: Error Measures for Parameter Influence

New Statistics

Monte Carlo: Error Measures for Parameter Influence (2)

F-statistic and p-value:
- New test statistic for R² being significantly >0 (small p is good).

R_adj² (Adjusted coefficient of determination):
- Takes number of samples and parameters into account
- Better suited than R² for comparing models on different subsets of process parameters
Monte Carlo: Sample Size Recommendation

Sample size $n$:
- $n < \text{number of stat.}$
- $\text{Param.} + 10$: no significant $R^2$-values or significant F-statistic
- $n < \text{number of stat. Param.} + 1$: t-statistic and confidence intervals cannot be calculated

Therefore, $n$ should be larger than the number of parameters +10.

Auto Synching

- Automatically synchronize simulation data and design history to disc
- Reduce risk of data loss
- Interval configurable
  - During runtime
  - Via configuration file (wicked-options.xml)
Call Application in Simulation Sub-Directory

- Execute any application in simulation sub-directory
- For easy debugging/inspection e.g. of failed simulation

**Supported Operating Systems**

- **Sun**
  - *Solaris 8, 9, and 10*

- **Linux**
  - *Default package (wicked5.2_linux.tar): Redhat Enterprise Linux (RHEL) 2.1, 3, and 4*
  - *Unsupported package (wicked5.2_linux_unsupported_rhel5.tar): RHEL 5*
New Features planned for 6.0

Overview

- Multiple top-level netlists („multi-testbench capability“)
  - Advanced matching capabilities
  - Easy setup of mismatch correlations between testbenches
- Support top-level („flat“) DUT for mismatch and constraints
- Mismatch simulation with unmodified Spectre model files
- Behavioral modeling
- Reduced memory consumption
- Optimization of GUI to improve speed (needed for large designs)
- Supported operating systems
- Availability: 1. half of 2008
Behavioral Modeling

- Extension of current analysis & optimization approaches to system-level (e.g. PLL) from block-level
- Typically, transistor-level simulation of analog & mixed-signal systems prohibitively costly (e.g. jitter of PLL)

⇒ Simulation time has to be reduced significantly

- Replace transistor-level representation of blocks with simpler macro models
- Requirements on macro-models
  - Capture important physical effects (e.g. influence of operating parameters and process variations) on circuit
  - Efficient generation and evaluation

⇒ Numerical macro models

Applications of Behavioral Models

**System model**
- Analog systems: PLL, ADC, DAC, ...
- Circuit blocks: Opamp, CCO, ...
- Circuit components: Transistors, resistors, ...

**Circuit model**
- Numerical model
  \[ \hat{y}(x) = \sum_{i=1}^{n_f} k_i \hat{f}_{bf,i}(x) \]

**ANALYSES**
- System level performances
- Circuit level performances
- Individual components (including parasitics)
MunEDA's Behavioral Modeling

- Automatic creation of behavioral models in Verilog-A or VHDL-AMS with consideration of:
  - Design parameters
  - Operating parameters
  - Process parameters
- Multiple algorithms for selection of model grid points:
  - Pre-defined or static selection
  - Dynamic selection (higher accuracy of model with similar simulation cost)
- And multiple basis functions:
  - Polynoms (generally good waveform matching)
  - Radial basis functions (generally better for local variations)
  - Automatic combinations of the above two
- Assessment of model accuracy

### Automatic Model Creation

1. Transistor-level circuit description
2. Selection of model parameter set
3. Selection of model grid points
4. Selection of basis functions
5. Model fitting
6. Model validation
7. OK?
8. Emit models in Verilog-A or VHDL-AMS
Selection of Model Grid Points

- Multiple options for selection of model grid points
  - Regular spacing
  - Random (Monte Carlo)
  - Latin Hypercube Sampling

- Adaptive methods for model improvement
  - Adaptive volume slicing
  - Adaptive cross slicing

Parameters of multiple basis functions may be used in the model:

- Polynomials
  \[ f_{bf,poly}(x) = \sum_i a_i \prod_j x_{ij}^k \]

- Radials
  - multiquadric
  - inverse multiquadric
  - Gaussian
  - thin-plate-spline
  - cubic
Supported Operating Systems

- Sun
  - Solaris 8, 9, and 10

- Linux
  - Default package (wicked6.0_linux.tar):
    Redhat Enterprise Linux (RHEL) 3, 4, and 5
  - Unsupported package (wicked6.0_linux_unsupported_rhel21.tar):
    RHEL 2.1
Automatic Analog Circuit Synthesis using WiCkeD

Xiaoying Wang
wang@em.informatik.uni-frankfurt.de

Johann-Wolfgang Goethe Universität Frankfurt am Main
www.em.informatik.uni-frankfurt.de

About Johann-Wolfgang Goethe Universität Frankfurt
The Institute for Computer Science works with the Chair for Electronic Design Automation (Prof. Lars Hedrich) as well as with the Chair for Technical Computer Science since long time in the field of design automation of microelectronic circuits. Main research topics are methods for the design and verification of analog circuits.

These topics divide into symbolic analysis, generation of behaviour models, synthesis and formal verification. In the area of equivalence-checking there is long-lasting cooperation with industrial partners, especially with Infineon Technologies. Since recent time the research group is also busy with the field of model-checking. Here methods for pure analog and mixed analog digital circuits will be developed. Symbolic analysis and behaviour model generation are basic topics, that will be required for formal methodologies but also for synthesis.
Automatic Analog Circuit Synthesis using WiCkeD

Xiaoying Wang
J.-W. Goethe University of Frankfurt, Germany

MunEDA User Group Meeting, Munich, Sept. 2007

Outline

• Introduction
• Automatic Analog Circuit Synthesis
  – Topology generation
  – Topology selection
  – Circuit sizing using WiCkeD
• Summary
Introduce

Institute of Computer Science, University of Frankfurt, Germany
Electronic Design Methodology Group with Prof. Hedrich (founded since 2004)

<table>
<thead>
<tr>
<th>EDA for analog circuits</th>
<th>Project</th>
<th>Theme</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formal verification</td>
<td>SAMS</td>
<td>Struktural Synthesis of Analog Circuits</td>
<td>Finished</td>
</tr>
<tr>
<td>Symbolic analysis</td>
<td>FEST</td>
<td>Model-checking of Nonlinear Circuits</td>
<td>Finished</td>
</tr>
<tr>
<td>Circuit synthesis</td>
<td>VeronA</td>
<td>Formal Verification of Analog Circuits</td>
<td>Started</td>
</tr>
<tr>
<td>Basic symbolic and numeric algorithms</td>
<td>Honey</td>
<td>Yield and Reliability Oriented Design Methods</td>
<td>Starting late 2007</td>
</tr>
<tr>
<td>Symbolic/numeric model library</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equivalence-checking</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Automatic behavioural modeling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sizing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Model-checking</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbolic analysis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Topology synthesis</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Design flow

Specification \{ gain, f_t, slew rate, etc. \} \[ \text{target} \]

Topology generation \{ Hierarchical synthesis \}

Topology selection \{ Symbolic analysis \}

Sizing \{ WiCkeD sizing tool \}

No. of circuits
Topology synthesis: state of the art

- **Topology library**
  - e.g. OASYS(89')

- **Topology generation**
  - with single transistor as building block
  - with genetic algorithms
    - DARWIN(95'), [Dastidar] (05')

```
I_z = I_{bias}
U = A*(U_+ - U_-)
```

Select-algorithms

Transistor netlist

Specification

Generation all possible structures

Selection/Evaluation

Transistor netlist

Hierarchical topology synthesis

- A set of well defined blocks with specialized signal information of terminals
- Synthesis rules for combination between blocks
- Block-chains/nets can represent the topology of circuits
- Generation instead of library: new circuits
Design example

• Block net:

```
+-------------------+-------------------+
| diff.-pair        |                   |
|                   |                   |
| U⁺                | U⁻                |
|                   |                   |
| +-------------------+-------------------+|
```

• Schematic

Topology Selection – Symbolic Analysis

• Goal of topology selection
  – Reduce high number of synthesized circuits
  – Short run time

• Symbolic analysis
  – Fast performance estimation
  – Performance ⇔ parameter dependencies
  – Simple design equations ⇒ Initial sizing
Symbolic Analysis – Work Flow

**topology generation**

**linear symbolic analysis**

- **set-up**
  - \( R_n^{\text{in}} + C_n \cdot X_n + R_n \cdot X_n = 0 \)
  - \( \beta \cdot x_n \cdot x_j' + x_i - U_n = 0 \)

- **simplify solve**
  - \( H(s) = \frac{g_m \cdot R_n}{1 + g_m} \cdot C \cdot s \)

**performance evaluation**

\[
\text{Performance} = f(W_1, \ldots, W_n, L_1, \ldots, L_n, I_{\text{bias}1}, \ldots, I_{\text{bias}n})
\]

with \( \forall i \ W_i = W_{\text{nom}} \),

- \( L_i = L_{\text{nom}} \),
- \( I_{\text{bias}1} = I_{\text{bias2nom}} \)

→ **compare to spec.**

Circuit sizing: WiCkeD

- **Sizing tool**: WiCkeD
- **Interface**: GUI or CLI?
  - **GUI**: graphical user interface
    - Interactive
    - User-friendly
    - Manuel command input
      → **few circuits**
  - **CLI**: command line interface
    - Non-interactive
    - Embedded into TCL
    - Efficiency and productivity
      → **more circuits**
CLI instead of GUI -- how?

- **Sizing flow in GUI**
  1. Circuit preparation
  2. Parameter setup
  3. Optimization / sizing

  ![Image of GUI flow](image)

- **CLI with command:** `wicked -s xxx.tcl xxx.def`

  - Files about:
    - circuit structure;
    - simulation info;
    - test bench;
  - Files about:
    - constrains;
    - specifications;
  - Files about:
    - sizing process;

---

Circuit sizing: design flow

- **topology generation**
- **symbolic analysis**

- Circuit structures
  - Feasibility Optimization
  - Nominal Optimization

- Testbench

- Sized circuits

- Specification: gain, \( f_c \), CMRR, power, etc..

---
Synthesis example – comparator (I)

• Synthesize comparator:
  – op + output stage

• Specifications:
  – High Slew-Rate > 5V/us
  – Load capacity = 1nF

• Result:
  – 4424 => 446 => 40 circuits

Synthesis example – comparator (II)

• Block chain:
  - Diff.- pair
  - Current mirror
  - Output stage

• Auto. gen. schematic:

• Performance:
  - Area: 70 \mu m^2
  - Gain: 67 dB
  - OutpVoltRange: 2.0 V
  - Ft: 9.9 MHz
  - Power: 7.4 mW
  - SlewF: 5.13 V/\mu s
  - SlewR: 5.36 V/\mu s
  - PSRR: 54.5 dB
  - CMRR: 41.8 dB
Summary

• Generation and selection of analog circuits step by step
  – Generation with hierarchical blocks
  – Fast symbolic analysis
  – Automatic sizing using WiCkeD CLI for a large number of circuits

• Outlook
  – More circuit classes

Thanks!
Integration of Statistical Sizing Methods
in Infineon Analog-Mixed-Signal-Flow

Dr. Eckhard Hennig
CAD Staff Engineer
eckhard.hennig@infineon.com
Infineon AG
www.infineon.com

About Infineon
Infineon Technologies AG, Munich, Germany, offers semiconductor and system solutions for applications in the wired and wireless communications markets, for security systems and smartcards, for the automotive and industrial sectors, as well as memory products. With a global presence, Infineon operates in the US from San Jose, CA, in the Asia-Pacific region from Singapore and in Japan from Tokyo, with about 33,800 employees worldwide. In the mobile radio area, Infineon Technologies is one of the leading suppliers of integrated circuits. Infineon has been participating in a variety of funding projects concerning EDA, so recently in SpeAC, ANASTASIA, MESDIE, ASDESE, LoMoSA, VISION, RapidMPSoC. Due to newest CMOS technology highly integrated solutions for cellular communication systems, local area systems, high performance data communication, and satellite navigational systems can be provided.
Integration of Statistical Design Methods into Infineon’s Analog/Mixed-Signal Design Flow

Dr.-Ing. Eckhard Hennig
EDA Staff Engineer
Infineon Automotive Power Division

MunEDA User Group Meeting 2007

Overview

- A/MS Design Flow Environment
- Statistical Device Model Implementation for Spectre and WiCkeD
- Statistical Process Modeling
Design-for-Yield Flow

Cadence Virtuoso
Schematic Editor + ADE

WiCkeD
Constraint Editor

Netlists & constraints

Device Parameters

WiCkeD
Sizing & Yield Analysis Engine

Backannotation

Circuit Simulator
Spectre, Titan

Performance Extraction
ocean, artil

Design point/parameter values

Performances

Job distribution via LSF

Waveforms

A/MS Design Flow: A Complex Environment for WiCkeD ...

Cadence Virtuoso

Simulation Environment

Design Framework

Tool Configuration

Design Flow Infrastructure

Stat. Device Models

Simulators

Netlist Formats

Spectre, Titan

Solaris, Linux

Operating Systems

IT Infrastructure

Job Distribution

Cadence DFII

ADE

Device Libraries

ATE
Overview

- A/MS Design Flow Environment
- Statistical Device Model Implementation for Spectre and WiCkéD
- Statistical Process Modeling

Statistical Device Model Implementation for Spectre and WiCkéD

Requirements

- Spectre device models must be implemented consistently for
  - native Monte-Carlo simulation with Spectre in Cadence ADE,
  - statistical analyses with WiCkéD/Spectre.

- To ensure consistency, a single Spectre model file set should be used.

Issues

- Mismatch parameter variation cannot be implemented identically for WiCkéD and native Spectre MC analysis.

→ See following slides for problem description and solution.
Statistical Model for MOSFET Threshold Voltage

- Threshold voltage is modeled as sum of
  - nominal value → constant
  - process variation → statistical variable with zero mean and process-specific standard deviation
  - mismatch variation → product of sigma(mismatch) and statistical variable dvth0 with zero mean and std. dev. = 1.

\[
V_{th0} = V_{th0,\text{nom}} + \Delta V_{th0,\text{process}} + \Delta V_{th0,\text{mismatch}}
\]

\[
\Delta V_{th0,\text{mismatch}} = \frac{dvth0}{\mu = 0, \sigma = 1} \cdot \sigma_{Vth0,\text{mismatch}}
\]

\[
\sigma_{Vth0,\text{mismatch}} = \frac{C_{Vth0,\text{mismatch}}}{\sqrt{2WL}}
\]

Statistical Model for MOSFET Carrier Mobility

- Mobility parameter is modeled as product of
  - nominal value → constant
  - process variation → 1 + statistical variable with zero mean and process-specific standard dev.
  - mismatch variation → product of sigma(mismatch) and 1 + statistical variable xmu0 with zero mean and std. dev. = 1.

\[
\mu_0 = \mu_{0,\text{nom}} \cdot \left(1 + \frac{\Delta \mu_{0,\text{process}}}{\mu = 0, \sigma = \sigma_{\mu0,\text{process}}} \right) \cdot \Delta \mu_{0,\text{mismatch}}
\]

\[
\Delta \mu_{0,\text{mismatch}} = \frac{(1 + x\mu0)}{\mu = 0, \sigma = 1} \cdot \sigma_{\mu0,\text{mismatch}}
\]

\[
\sigma_{\mu0,\text{mismatch}} = \frac{C_{\mu0,\text{mismatch}}}{\sqrt{2WL}}
\]
Statistical Device Modeling Implementation for Native Spectre Monte-Carlo Analysis

**inline subckt** nmos (d g s b)  
// Subcircuit instance parameters  
**parameters** w=1 l=1 mult=1  

...  
+ mmarea = sqrt(2*w*l*mult) // Area factor for mismatch  
+ mc_vth0 = nmos_vth0_nom + nmos_vth0_prc + nmos_vth0_mat*nmos_vth0_cmatch/mmarea  
+ mc_u0 = nmos_u0_nom*(1 + nmos_u0_prc) * (1 + nmos_u0_mat)*nmos_u0_cmatch/mmarea  

// Device model card  
**model** nmos_model bsim3v3 type = n version = 3.1  
+ ...  
+ vth0 = mc_vth0  
+ u0 = mc_u0  
+ ...  

// Inline device instance  
nmos (d g s b) nmos_model w=w l=l m=mult  
ends

Statistical Parameter Definition for Spectre

**parameters**  
+ nmos_vth0_nom = 0.78 // Nominal threshold voltage Vt [V]  
+ nmos_vth0_prc = 0 // Vt process variation [V] (zero mean)  
+ nmos_vth0_mat = 0 // Vt mismatch variation [1] (zero mean)  
+ nmos_vth0_cmatch = 4n // Vt matching constant [μm V]  
+ nmos_u0_nom = 650 // Nominal carrier mobility μ0 [cm²/Vs]  
+ nmos_u0_prc = 0 // μ0 process variation [1] (zero mean)  
+ nmos_u0_mat = 0 // μ0 mismatch variation [1] (zero mean)  
+ nmos_u0_cmatch = 5n // μ0 matching constant [μm]  

**statistics** {  
  **process** { // Process variations: zero mean, absolute sigma  
    vary nmos_vth0_prc  dist = gauss  std = 0.01  
    vary nmos_u0_prc  dist = gauss  std = 0.02  
  }  
  **mismatch** { // Normalized mismatch variations: zero mean, sigma = 1  
    vary nmos_vth0_mat  dist = gauss  std = 1  
    vary nmos_u0_mat  dist = gauss  std = 1  
  }  
}
Referencing Statistical Device Models in Spectre Netlists

- Device instance statement in Spectre netlist for native Monte-Carlo analysis:

  M1 (1 2 3 VSS!) nmos w=1u l=200n

  → Mismatch parameters are varied internally by Spectre for each instance of nmos.

- Device instance statement in Spectre netlist for WiCkeD requires explicit mismatch parameter passing for each Monte-Carlo sample:

  M1 (1 2 3 VSS!) nmos w=1u l=200n \
  dvth0=0.2761 xmu0=-0.1628

WiCkeD-Compatible Mismatch Modeling (1)

```plaintext
inline subckt nmos (d g s b) // Subcircuit instance parameters
parameters w=1 l=1 mult=1
... + mmarea = sqrt(2*w*l*m) // Area factor for mismatch
+ mc_vth0 = nmos_vth0_nom + nmos_vth0_prc + nmos_vth0_mat*nmos_vth0_cmatch/mmarea
+ mc_u0 = nmos_u0_nom*(1 + nmos_u0_prc) * (1 + nmos_u0_mat)*nmos_u0_cmatch/mmarea

// Device model card
model nmos_model bsim3v3 type = n version = 3.1
+ ...
+ vth0 = mc_vth0
+ u0 = mc_u0
+ ...

// Inline device instance
nmos (d g s b) nmos_model w=w l=l m=mult ends
```

Mismatch variables must be global parameters. Spectre does not allow them to be subckt instance parameters.

This does not work!
WiCkeD-Compatible Mismatch Modeling (2)

**inline subckt** nmos (d g s b)

**parameters**

w=1  l=1  mult=1

...  
+  dvth0  =  0  // Vt mismatch parameter for WiCkeD
+  xmu0  =  0  // \( \mu \) mismatch parameter for WiCkeD
+  mmarea  =  sqrt(2*w*l*m)  // Area factor for mismatch
+  mc_vth0  =  nmos_vth0_nom + nmos_vth0_prc +
  (dvth0==0?nmos_vth0_mat:dvth0)*nmos_vth0_cmatch/mmarea
+  mc_u0  =  nmos_u0_nom*(1 + nmos_u0_prc) *
   (1 + (xmu0==0?nmos_u0_mat:xmu0))*nmos_u0_cmatch/mmarea

**model** nmos_model bsim3v3 type = n  version =

+  ...
+  vth0  =  mc_vth0
+  u0  =  mc_u0
+  ...

nmos (d g s b) nmos_model  w=w  l=l  m=mult  

**ends**

**Solution**

WiCkeD mismatch parameters are effective only if they are explicitly set to a non-zero value in the netlist, otherwise Spectre parameters \_*mat are used.

**Note:** solution works also for mismatch parameters with non-zero mean.

Overview

- A/MS Design Flow Environment
- Statistical Device Model Implementation for Spectre and WiCkeD
- Statistical Process Modeling
NMOS Vt over a period of 30 days

Lower PCM Specification Limit (LSL)

Process Target

Upper PCM Specification Limit (USL)

Count

0.7 0.8 0.9

This Month

Last Month
Statistical Process Modeling: Basic Philosophy

- Accurate yield prediction with WiCkeD requires precise statistical process modeling.

... But ...

- Manufacturing processes often exhibit some drift over time.
- Gathering reliable statistical data requires long-term process observation (months ... years) – not possible during process development and lead product design.

... Therefore ...

Statistical Process Modeling: Basic Philosophy

  - Less sensitive to process drift.
  - Enhanced corner analysis rather than accurate yield prediction.

\[
\begin{align*}
\text{NMOS } V_t & \text{ over a period of 30 days} \\
\text{Lower PCM Specification Limit (LSL)} & \quad \text{Process Target} \quad \text{Upper PCM Specification Limit (USL)}
\end{align*}
\]

\[
V_{T, \text{nom}} := V_{T, \text{target}} \quad \sigma := \frac{\text{USL} - \text{LSL}}{6}
\]

\[
\begin{align*}
\text{Count} & = 3\sigma \\
\text{Norm. distribution} & := 3\sigma
\end{align*}
\]
We commit.
We innovate.
We partner.
We create value.
Analysis and Optimization of a CMOS Mixer Circuit

About Fraunhofer IIS EAS
Corresponding to the FhG’s R&D mission, the Dresden Division Design Automation (EAS) deals primarily dealt with working out practice relevant problems of Applied Research ordered by industry and the public authorities. Usually, these demanded activities are performed in cooperation with the customers, other industrial partners and competent R&D institutions.

Within the framework of funded R&D projects we mainly develop: methods and tools for CAD of electronic and heterogeneous systems.
In particular, these results are focussed on bridging dedicated gaps in application specific design flows and considerably improving the functionality and performance of commercially available CAD systems. Moreover, EAS has been involved in the design and verification of prototyping of hardware software systems for years.

The R&D results are required for innovative applications in Telecommunications, Digital Radio (DAB, DVB) and also for the development of micro-systems.
Analysis and optimization of a CMOS mixer circuit

Ronny Frevert, Uwe Knöchel, Thomas Markwirth
Fraunhofer Institut Integrierte Schaltungen,
Institutsteil Entwurfsautomatisierung, Dresden

Matthias Sylvester
MunEDA GmbH, München

Content

1. Introduction and motivation
2. Example circuit, initial sizing and simulation results
3. WiCkeD Constraint Editor settings
4. Analysis and optimization flow
5. Results and outlook
Introduction and motivation

— since 2006 cooperation between MunEDA and Fraunhofer
— successful test of WiCkeD at a bandgap circuit
— preparation of an RF circuit example:

CMOS mixer circuit

Challenges of the mixer optimization

— special RF analyses required, e.g. Periodic Steady State analysis (PSS) and Periodic small-signal analyses
— the application of OCEAN postprocessing functions to calculate mixer performances, like noise figure or intercept points

Introduction to the Gilbert Cell mixer

— picture shows a double-balanced mixer, also called Gilbert Cell
— the Gilbert Cell mainly consists of 3 differential pairs
— the small RF signal is applied to M5,M6
— the large LO signal is applied to M1,M2 and M3,M4
— by turning M1,M2 and M3,M4 on and off, the RF signal is mixed to the intermediate frequency (IF)
— Advantages: LO and RF are both balanced, good port-to-port isolations, high intercept points
— Disadvantages: high LO level required, high power supply
Characterization of a mixer

Important performances and required analyses

<table>
<thead>
<tr>
<th>Mixer performance</th>
<th>Analysis (Cadence ADE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Harmonic distortion</td>
<td>Periodic Steady State (PSS)</td>
</tr>
<tr>
<td>S-Parameters</td>
<td>PSS and Periodic S-Parameter (PSP)</td>
</tr>
<tr>
<td>Noise figure</td>
<td>PSS and PNoise</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>PSS and Periodic Transfer Function (PXF)</td>
</tr>
<tr>
<td>Port-to-Port isolations</td>
<td>PSS and Periodic AC (PAC)</td>
</tr>
<tr>
<td>1dB Compression Point</td>
<td>Swept PSS</td>
</tr>
<tr>
<td>2nd/3rd order Intercept Point</td>
<td>Swept PSS</td>
</tr>
<tr>
<td>Power consumption</td>
<td>PSS or DC</td>
</tr>
</tbody>
</table>

Difficulties

— no unique testbench, that fits for all performances
— different configuration of the analyses are required but not allowed within the same Artist session
— due to this limitation no full optimization of the mixer is available with IC5.1 and WiCkeD 5.0

Content

1. Introduction and motivation
2. Example circuit, initial sizing and simulation results
3. WiCkeD Constraint Editor settings
4. Analysis and optimization flow
5. Results and outlook
Example circuit and initial sizing

- the CMOS mixer is based on the Gilbert Cell topology
- it consists of:
  - the Gilbert Cell
  - a current mirror
  - resistors and capacitors
- all NMOS transistors
  \[ W=230\mu, \ L=600\text{n} \] (ex. M7)
- load resistors (R1, R2)
  \[ W=3.5\mu, \ L=1\mu \ (500 \Omega) \]
- source resistors (R3, R4)
  \[ W=180\mu, \ L=1\mu \ (10 \Omega) \]
- input resistors (R5, R6)
  \[ W=1\mu, \ L=9.6\mu \ (10 \text{k}\Omega) \]

Testbench

The testbench consists of:

- the mixer DUT
- three baluns
- ports and sources

Frequencies:

- \( f_{RF} = 2.5 \text{ GHz} \)
- \( f_{LO} = 2.75 \text{ GHz} \)
- \( f_{IF} = 250 \text{ MHz} \)

Sources:

- \( vdc = 2.5 \text{ V}, \ idc = 600 \mu\text{A}, \ alo = 600 \text{ mV} \)
Simulation results before optimization

**Conversion gain = 6.97 dB**
- measured with PSS/ PXF
- \( f_{\text{in}} = f_{\text{out}} + k_i \cdot f_{\text{PSS}} \)
- \( f_{\text{PSS}} = f_{\text{LO}} = 2.75 \) GHz
- \( k_i = -1 \) (lower sideband)
- \( f_{\text{out}} = f_{\text{IF}} = 250 \) MHz
- \( f_{\text{in}} = -2.5 \) GHz

OCEAN measurement: \( \text{value(db(harmonic(getData("/PORT0" ?result "pxf") '-1)) 250M)} \)

Simulation results before optimization

**Noise figure = 13.45 dB**
- measured with PSS/PNoise
- \( |f_{\text{in}}| = |f_{\text{out}} + \text{refsideband} \cdot f_{\text{PSS}}| \)
- \( f_{\text{PSS}} = f_{\text{LO}} = 2.75 \) GHz
- \( \text{refsideband} = -1 \)
- \( f_{\text{out}} = f_{\text{IF}} = 250 \) MHz
- \( f_{\text{in}} = 2.5 \) GHz

OCEAN measurement: \( \text{value(getData("NF" ?result "pnoise") 250M)} \)
Simulation results before optimization

Power consumption = 25.11 mW
— measured with DC analysis
— power of the LO signal is not included

OCEAN measurement: abs((i("/V7/PLUS" ?result "dcOp") * v("/net037" ?result "dcOp")))

Content

1. Introduction and motivation
2. Example circuit, initial sizing and simulation results
3. WiCkeD Constraint Editor settings
4. Analysis and optimization flow
5. Results and outlook
WiCkeD Constraint Editor settings

Design and Op. Parameters:
- temp: from -20 °C up to 50 °C
- vdc: from 2.4 V up to 2.6 V

Constraints:
- nSat for differential pair M5, M6 is disabled

Performance specifications:
- conversion gain > 8 dB
- noise figure < 13 dB
- power consumpt. < 50 mW

Content

1. Introduction and motivation
2. Example circuit, initial sizing and simulation results
3. WiCkeD Constraint Editor settings
4. Analysis and optimization flow
5. Results and outlook
Analysis and Optimization flow

Simulation results:
— two performance specifications (conversion gain and noise figure) are not fulfilled

Feasibility Optimization:
— one violated constraint in the current mirror
— optimization successful after two iterations
Analysis and Optimization flow

Nominal Optimization:
— Conversion gain and noise figure are outside the specification bounds
— A previous sensitivity analysis showed that the L’s of the differential pairs have the most influence on conversion gain and noise figure
— After one iteration the optimization is successful

Worst-Case Analysis:
— Yield after Nominal Optimization between 79% and 100%
— Improvement is necessary
Analysis and Optimization flow

Yield Optimization:
- Yield can be increased up to 100% (WCD > 3σ) after 4 iterations

Monte Carlo Analysis:
- Monte Carlo Analysis confirms the results of the Yield Optimization
Content

1. Introduction and motivation
2. Example circuit, initial sizing and simulation results
3. WiCkeD Constraint Editor settings
4. Analysis and optimization flow
5. Results and outlook

Results and Outlook

- Optimization of the CMOS mixer was successful
- All selected performances fulfill the specification
- Yield can be increased up to 100%
- Special RF analyses and OCEAN postprocessing functions can be used with WiCkeD
- The complete characterization and optimization of a mixer circuit requires multiple testbenches/multiple analyses of the same type and is not supported in the current version
- Cadence IC6.1 shall be evaluated if it supports this in future
PLL Hierarchical Optimization Methodology
Considering Jitter, Power and Locking Time

About Qimonda AG
Qimonda is a leading global memory supplier with a broad diversified DRAM product portfolio. The company generated net sales of €3.81 billion in its 2006 financial year and has approximately 13,000 employees worldwide. Qimonda has access to five 300mm manufacturing sites on three continents and operates six major R&D facilities. The company provides DRAM products for a wide variety of applications, including in the computing, infrastructure, graphics, mobile and consumer areas, using its power saving technologies and designs.

About Technische Universität München
The Institute for Electronic Design Automation at Technische Universität München (TUM-EDA) was founded in 1975 as the first research institute in Germany in the area of computer-aided design of electronic circuits. For many years, the institute has covered a broad scope of electronic design automation for digital and analog circuits. In the areas of logic synthesis, test design, layout synthesis, analog design and logic simulation, internationally renowned algorithms have been developed and transferred into industrial application.

TUM-EDA cooperates and competes with international universities like KU Leuven, Carnegie Mellon University, University of California at Berkeley, University of Sevilla. TUM-EDA cooperates with semiconductor companies like Infineon, Philips, Bosch, Atmel. Currently, TUM-EDA conducts research in three fields. In the area of statistical design of analog ICs, algorithms and tools for statistical analysis and design centering of analog circuits have been developed and transferred into practical application. They cover worst-case analysis, yield analysis, circuit sizing with operating conditions, yield optimization/design centering considering local and global process variations.

The developed tools are using external simulation. The corresponding tool suite WiCkeD has been commercialized by the TUM spin-off MunEDA (www.muneda.com). Among the users of WiCkeD are Infineon and ST Microelectronics. The preparation of analog test has also been a topic of research in this group. A second field of research is layout synthesis, in particular placement, where the methods of TUM-EDA (GORDIAN, KRAFTWERK) are incorporated in many tools worldwide. Our placer KRAFTWERK recently won the placement contest at ISPD. One of the current research projects deals with the automation of analog layout placement. Further research work takes place in the area of statistical design of digital circuits, specifically in statistical gate delay modeling, modeling of structure- and layout-induced correlations and propagation of delay distributions.
A Hierarchical Optimization Method for Phase-Locked Loops considering Jitter, Power and Locking Time

J. Zou
Qimonda AG

D. Mueller, H. Graeb, U. Schlichtmann
Institute for Electronic Design Automation
Technische Universitaet Muenchen

@ACM/IEEE Design Automation Conference (DAC) 2006

Outline

• Phase-locked loop
• Flat vs. hierarchical optimization
• Requirements of hierarchical optimization
• Result
Phase-Locked Loop (PLL)

- Clock generation, phase recovery

PLL on Transistor Level

externally biased CP

5-stage ring VCO
PLL System Performance

To be optimized:
- Power consumption: $P_{\text{sum}}$ (mW)
- Locking time: $T_s$ (μs)
- Jitter: $J_{\text{sum}}$ (ps)

Subject to:
- Output frequency range: $F_{\text{out}}$ (MHz)
- Phase margin (linear lock-in state stability): PM (°)
- Reference signal frequency to Unity-gain-bandwidth Ratio (nonlinear locking process stability): $RUR$
Flat Optimization Approach

- Overall system simulation on transistor level: large simulation effort

<table>
<thead>
<tr>
<th>Transistor level</th>
<th>#simulations</th>
<th>e.g. 200</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.5 h</td>
<td>12.5 days</td>
</tr>
<tr>
<td></td>
<td>6 h</td>
<td>50 days</td>
</tr>
</tbody>
</table>

- Overall model of system and its blocks including transistor-level parameters: large modeling effort
  - [Li, Wang, Pileggi, Chen and Chiang, ICCAD 2005]
  - [Hershenson, ICCAD 2002]
Hierarchical Optimization Approach

- Optimization engine
- Behavioral-level simulation of system
- Optimization engine
- Transistor-level simulation of block
- System performance
  - Behavioral-level sizing
  - Transistor-level block parameters, i.e. transistor-level block performance
  - Transistor-level sizing for each block

PLL on Behavioral Level

- Behavioral models of building blocks: moderate modeling effort
Hierarchical Optimization Approach

- Overall system simulation on behavioral level: moderate simulation effort

<table>
<thead>
<tr>
<th>Behavioral level</th>
<th>1 simulation</th>
<th>200 simulations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locking Time</td>
<td>40 sec</td>
<td>2.2 h</td>
</tr>
<tr>
<td>Jitter</td>
<td>2 min</td>
<td>6.6 h</td>
</tr>
</tbody>
</table>

- Two-stage process of top-down specification propagation from behavioral level to transistor level
  - [Eeckelaert, McConaghy & Gielen, DATE 2005]
  - [Tiwary, Velu, Rutenbar and Mukherjee, Nanotech 2004]
  - [Stehr, Graeb and Antreich, ICCAD 2004]

Outline

- Phase-locked loop
- Flat vs. hierarchical optimization
- Requirements of hierarchical optimization
- Result
Hierarchical Optimization Approach - Requirements

1. Behavioral models of building blocks parameterized according to block performance features
2. Prevent behavioral-level sizing from producing unrealistic requirements on transistor-level sizing: Pareto front
Top-Down Specification Propagation

specs on PLL system performance

CP

\( P_{sum} \), \( T_s \), \( J_{sum} \), \( F_{out} \), \( PM \), \( RUR \)

specs on transistor-level performance

IB, JCP

\( R_{LP} \), \( C_{LP} \), \( C_{LP2} \)

Behavioral-level parameter values

VCO

\( K_{VCO} \), \( J_{VCO} \), \( I_{VCO} \), \( F_{out} \)

Behavioral-level parameter values

\( w_{1CP}, l_{1CP} \), \( w_{1VCO}, l_{1VCO} \)

Transistor-level parameter values

Hierarchical Optimization Approach - Requirements

1. Behavioral models of building blocks parameterized according to block performance features

2. Prevent behavioral-level sizing from producing unrealistic requirements on transistor-level sizing: Pareto front
Pareto Front of Charge Pump’s Jitter vs. Current

\[
J_{cp} = a + b \cdot I_B + c \cdot I_B^{1.5} + d \cdot I_B^{0.5}
\]

I_{min} \leq I_B \leq I_{max} as constraint for behavioral-level sizing

Pareto Front of VCO’s Gain vs. Jitter vs. Current

\[J_{VCO} = f(I_{VCO}, K_{VCO})\]

(k_{VCO}, I_{VCO}) \in D as constraint for behavioral-level sizing
Hierarchical Optimization Approach

Behavioral modeling
1) Parameterized behavioral model
2) Pareto front

CP, VCO

Behavioral-level sizing

Pareto-front computation

CP, VCO

Transistor-level sizing

CP, VCO

Outline

- Phase-locked loop
- Flat vs. hierarchical optimization
- Requirements of hierarchical optimization
- Result
Hierarchical Optimization – Stage 1

- Simultaneous sizing of blocks' performance according to PLL performance specification
- PLL simulation on behavioral level

**PLL performance specification**
- Frequency: 150...500MHz
- Locking time: ≤ 2.5μs
- Jitter: ≤ 2.5ps
- Power: ≤ 2.5mW
- Phase margin: $\varphi \geq 60^\circ$

**VCO performance**
- Gain: 350MHz/V
- Current: 47μA
- Jitter: 13ps

**LF performance**
- $R$: 17kΩ
- $C_1$: 45pF
- $C_2$: 8pF

Hierarchical Optimization – Stage 2

- Concurrent sizing of blocks' parameters according to block performance specification
- CP, VCO simulation on transistor level

**CP performance**
- Current: 47μA
- Jitter: 13ps

**VCO performance**
- Gain: 350MHz/V
- Current: 620μA
- Jitter: 1.9ps

**CP parameters**
- $W$’s/$L$’s

**VCO parameters**
- $W$’s/$L$’s
### CPU Time

| Block Pareto fronts + | CP: about 1 hour  
| VCO: about 4-5 hours |
|-----------------------|------------------|
| Behavioral-level sizing + | about 1-2 hours |
| Circuit-level sizing = | CP: about 10 mins  
| VCO: about 1 hour |

---

Overall: about 8 hours

---

### Applied Methods and Tools

**Pareto fronts**  
[Mueller, Stehr, Graeb, Schlichtmann, DAC 2005]

**Sizing**
- Optimizer: WiCkeD  
  - [www.muneda.com](http://www.muneda.com)
- Optimizer: WiCkeD

**Simulation**
- Calculator: Octave  
  - [www.octave.org](http://www.octave.org)
- Simulator: Spectre  
  - [www.cadence.com](http://www.cadence.com)
- Simulator: Spectre
Conclusion

- Design of complex analog circuits requires a mixed-level modeling
- This leads to a two-stage optimization process
- Which can be implemented with an optimization tool like WiCkeD
- Enhanced by Pareto optimization
Challenges in Analog/Mixed-Signal EDA

About TU Ilmenau
The Technische Universität Ilmenau occupies a top position both nationally and internationally in a number of areas of research, pure and applied. It has been possible to establish highly competitive research activities, particularly by relying upon interdisciplinary work across faculty boundaries and the bringing together of many skills that that implies.

The Senate of the Technische Universität has decided upon the following main foci with the aim of giving the University an unmistakeable profile with unique features:

- Micro- and nano- systems
- Stationary and mobile intelligent systems
- Innovative communication and media systems
Challenges in Analog/Mixed-Signal EDA

Ralf Sommer & Dominik Krauße

Fakultät EI, Fachgebiet “Elektronische Schaltungen und Systeme”
Univ. Prof. Dr.-Ing. Ralf Sommer
Dienstzimmer: Helmholtzbau, Zimmer 3511
Telefon: 03677-69 2624
Telefax: 03677-69 1163
E-mail: ralf.sommer@tu-ilmenau.de
http://www.tu-ilmenau.de/site/se_ess/index.php?id=836

Univ. Prof. Dr.-Ing. Ralf Sommer
wissenschaftlicher Geschäftsführer
IMMS gGmbH
Tel.: 03677-69 5500
Fax.: 03677-69 1163
Ehrenbergstraße 27
D-98693 Ilmenau
http://www.imms.de ralf.sommer@imms.de

Curriculum vitae
Ralf Sommer (Ralf.Sommer@imms.de)

- **Technical University of Braunschweig (Germany)**
  - Study of electrical engineering – network theory and micro-electronics
  - Ph.D.: "Concepts and methodologies for the computer-aided design of analog circuits"

- **University of Kaiserslautern / Fraunhofer ITWM (Germany)**
  Director of the project "Computer-aided Design of Analog Circuits (EDA-electronic design automation)", development of the commercial symbolic analysis tool "Analog Insydes"

- **Infineon Technologies AG, Munich (Germany)**
  Group leader "Analog Simulation Group" and jointly responsible in Infineon research activities "Design Automation" in the central CAD department

- **Technical University of Ilmenau & IMMS gGmbH (Germany)**
  Professor “Electronic Circuits and Systems” at TUI and scientific director of the Institute of Microelectronic and Mechatronic Systems gGmbH
Outline

- IMMS – overview & fields of competences
- Design and optimization of a transimpedance amplifier circuit
- Aging
- Hierarchy and behavioral modeling
- Multi-domain modeling
- Topics for innovation activities in EDA

Structure of IMMS

- Founded in 1995 / 1997 opening of the Erfurt branch office
- Institute of the state of “Thuringia”
- Since 1998 “Associated Institute of the Technical University of Ilmenau” (An-Institut)
- Budget in 2006 → approx. 4.2 Million Euros
- Currently 69 employees
- approx. 25 student internships / graduates / graduate assistants
Departments of IMMS

Application of industry-oriented Research and Development

System Design
- Buses and networked systems
- Embedded software
- Automotive Systems
- Digital signal processing / Industrial Electronics

Mechatronics
- Precision drive systems
- Drives for UHV-applications
- Devices for analysis
- Complex mechatronical systems

Circuit Technology
- Optoelectronics
- Sensor-Interfaces
- RF-Design
- Mixed-signal ASICs
- Modeling and simulation
  → Design methodology & EDA

Analysis & Testing
- Testing ASICs
- Design support
- RF-measurement
- Opto measurements
- Non-standard measurement

Classification of Competences: From Circuit to System

Modeling, Simulation, Design, Analysis, Test, Prototyping, Consulting, Documentation, ...

Problem / Specification from the customer

Research project
Industrial project
Combined project

Device / Module / Schematic
Circuit
PCB Module
Functional unit
Equipment

... complete, complex, custom-specific solution/service performance interdisciplinary worked out
Design Steps System → Analog/Mixed-Signal Circuit

**System concept/Circuit**

- selection of components
- topology selection
- sizing
- cell-level layout
- system layout

- no analog circuit synthesis
- many iterations
- complex dependencies, feedback, parasitic effects

Design Steps in Mechatronics

**Machine concept**

- System design, selection of components
- Sizing and simulation
- domain-specific design of subblocks
- System design, -integration

- complex synthesis (mechanics, electronics, control systems)
- many iterations
- complex dependencies, feedback, parasitic effects
Research Topics – IMMS Erfurt

- Circuit and system design
  - Analog and mixed-signal circuit design: TI Amps, Op Amps, SC circuits, ADC
  - Optoelectronics, photo diodes and optical busses
  - RF circuit design and calibration

- Design methods
  - New design methods for A/MS
  - Design centering and symbolic analysis
  - Formal verification

- New technologies of MEMS, SOI, smart power and high temperature
- Micro mechanical and sensor systems
- Modeling and Design Kits, ESD

Blue DVD Pick-Up Systeme

<table>
<thead>
<tr>
<th>TV/DVD</th>
<th>HDTV</th>
</tr>
</thead>
<tbody>
<tr>
<td>720 x 483</td>
<td>1900 x 1080</td>
</tr>
</tbody>
</table>

Picture:
- larger, sharper, faster

Technology:
- smaller, cheap, long-lasting, intelligent, comfortable, more features
An Old & Well-known Slide from ANASTASIA+ Project
Top-Down Designflow – Still a Challenge

Analog
Mixed
Signal
Digital
Semi Custom
Digital
Full Custom

MunEDA User Group Meeting: Challenges in Analog/Mixed-Signal EDA

Analog Block Design with Topology Reuse:
From Block Specification to Sized Circuit Topology

- Gain
- Slew Rate
- ...
Simulation Results before Optimization

**Ringing in Transient Plot**

**Peaking in Bode Plot**

MunEDA User Group Meeting: Challenges in Analog/Mixed-Signal EDA

15.09.2007

**Optimization Goals**

<table>
<thead>
<tr>
<th>Performance</th>
<th>Spec</th>
<th>Before optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>3dB bandwidth</td>
<td>&gt; 250 MHz</td>
<td>419 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>&gt; 60°</td>
<td>-180°</td>
</tr>
<tr>
<td>Slew rate rising</td>
<td>&gt; 400 V/μs</td>
<td>1100 V/μs</td>
</tr>
<tr>
<td>Slew rate falling</td>
<td>&lt; - 400 V/μs</td>
<td>- 532 V/μs</td>
</tr>
<tr>
<td>Peaking (Bode plot)</td>
<td>&lt; 1 dB</td>
<td>8 dB</td>
</tr>
<tr>
<td>Offset</td>
<td>&lt; ±1 mV</td>
<td>727.9 μV</td>
</tr>
<tr>
<td>DC gain</td>
<td>&gt; 83 dB</td>
<td>83.9 dB</td>
</tr>
</tbody>
</table>
Global Optimization

Failed performances in Global Optimization

Deterministic Optimization

Failed performances in Deterministic Optimization
Simulation Results after Optimization

Global Optimization

Deterministic Optimization

Circuit Performances

<table>
<thead>
<tr>
<th>Performance</th>
<th>Spec</th>
<th>Before optimization</th>
<th>After deterministic optimization</th>
<th>After global optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>3dB bandwidth</td>
<td>&gt; 250 MHz</td>
<td>419 MHz</td>
<td>431 MHz</td>
<td>224 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>&gt; 60°</td>
<td>-180°</td>
<td>0°</td>
<td>47.6°</td>
</tr>
<tr>
<td>Slew rate rising</td>
<td>&gt; 400 V/μs</td>
<td>1100 V/μs</td>
<td>1000 V/μs</td>
<td>266 V/μs</td>
</tr>
<tr>
<td>Slew rate falling</td>
<td>&lt; - 400 V/μs</td>
<td>- 532 V/μs</td>
<td>- 500 V/μs</td>
<td>- 406 V/μs</td>
</tr>
<tr>
<td>Peaking (Bode plot)</td>
<td>&lt; 1 dB</td>
<td>8 dB</td>
<td>2.8 dB</td>
<td>2.6 dB</td>
</tr>
<tr>
<td>Offset</td>
<td>&lt; ±1 mV</td>
<td>727.9 μV</td>
<td>- 872 μV</td>
<td>- 6.6 mV</td>
</tr>
<tr>
<td>DC gain</td>
<td>&gt; 83 dB</td>
<td>83.9 dB</td>
<td>83.9 dB</td>
<td>83.8 dB</td>
</tr>
</tbody>
</table>
Conclusion

- Neither deterministic nor stochastic optimization succeeded in fulfilling the specs
- Change of topology?
  - apply symbolic analyses to determine AC parameters allowing to change position of critical poles and zeros
  - apply new methodology for systematic topology changes
  - optimize parameter values using WiCkeD

Principle of Direct Frequency Compensation: Laplace – Domain Interpretation

- |H(s)|
- poles
- zeros
- frequency-response |H(s = jω)|
- line of critical damping (Re = Im)
Direct Frequency Compensation with Analog Insydes

- Determine approximate transfer function with Analog Insydes to extract/keep dominant parameters
- Find transistor capacitances (e.g. cbe, cbc, cgs …) that have a proper influence on the pole-zero locations
- In schematic, connect a capacitor in parallel to the transistor capacitance and analyze behavior/performance
New Methodology for Extended Topology Modification

- Connect capacitors (also R-C possible) from each node of the network to the others
- Check the pole/zero plot for proper influences on the poles
  → **Note:** This method increases computation time on larger circuits (use symbolic approximation for speedup)
- Update schematic with suitable capacitances
- Analyze the circuit with parametric sweeps on each new capacitor→ find an optimum solution (WiCkeD)

Root-Locus Plot: Introducing a New Capacitance
Pole zero plot with capacitance sweep

Increasing capacitance

Transient Plot after Compensation

<table>
<thead>
<tr>
<th>Performance</th>
<th>Before optimization</th>
<th>After compensation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peaking</td>
<td>8 dB</td>
<td>0.74 dB</td>
</tr>
</tbody>
</table>
### Simulation Results

<table>
<thead>
<tr>
<th>Performance</th>
<th>Spec</th>
<th>Simulation result</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(Capacitance 40 pF)</td>
</tr>
<tr>
<td>3dB bandwidth</td>
<td>&gt; 250 MHz</td>
<td>255 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>&gt; 60°</td>
<td>73°</td>
</tr>
<tr>
<td>Slew rate rising</td>
<td>&gt; 400 V/µs</td>
<td>653 V/µs</td>
</tr>
<tr>
<td>Slew rate falling</td>
<td>&lt; - 400 V/µs</td>
<td>- 515 V/µs</td>
</tr>
<tr>
<td>Peaking (Bode plot)</td>
<td>&lt; 1 dB</td>
<td>0.74 dB</td>
</tr>
<tr>
<td>Offset</td>
<td>&lt; ±1 mV</td>
<td>727.9 µV</td>
</tr>
<tr>
<td>DC gain</td>
<td>&gt; 83 dB</td>
<td>83.9 dB</td>
</tr>
</tbody>
</table>

Will the circuit work tomorrow?
Device Degradation Effects

- NMOS Hot Carrier Injection (HCI) Effect
  - $E_{\text{max}}$ at drain corner causes hot carrier generation
  - Hot carriers cause $I_{\text{sub}}$, $I_{\text{gate}}$ and oxide damages

Thanks to H. Nielen, Infineon
HCl: Degraded NMOS Id-Vds Characteristics

- Lower current drivability = slower circuits!
- Gm degradation and Vt shift are big issues for analog applications!

![Graph showing NMOS Id-Vds Characteristics]

Device Degradation Effects

- NBTI (Negative Bias Temperature Instability)
  - Hydrogen-silicon bond (Si-H) is broken
  - Hydrogen is trapped into the oxide → interface trap
  - Shift of threshold voltage (Vt)
  - Dominating in P-MOSFET
  - More dominating than HCl in current processes

![Diagram of NBTI effect on MOSFET]

Parametric shift
- Increase of Vth
- Decrease of g_m
- Increase of Ioff
- Decrease of I_dsat
NBTI: Temperature Dependency

![Graph showing DeltaId/Id vs Time vs Temp](image)

- T = 27°C
- T = 85°C
- T = 125°C

Reliability Assessment

- **Conventional approach:**
  - Clarify the **most critical circuits/transistors + conditions**
  - Clarify the **most interesting degradation parameter** (e.g.: \( \text{Idsat} \) or \( \text{Idlin} \) or \( \text{Vth} \))
  - **Best guess** about the corresponding critical degradation limit (e.g.: \( \Delta \text{Idsat} = 10\% \))

![Graph showing Id vs Vds](image)

- before stress
- after stress
- degradation of Idsat

pass or fail

Thanks to H. Nielen, Infineon
AGEMOS Model Extraction

(adding degradation statements to transistor model cards)

- Goal: describe the change of the (individual) BSIM transistor models due to device degradation:
  - $\Delta$BSIM-Par = f(age, load/stress)

---

DfR - RelXpert Simulation Flow

- Fresh Simulation
  - Duty cycle incl. $I_{sub}$

- Simulation 1
  - Circuit implementation
  - Aging information for each single transistor inside the circuit
  - Flat netlist with individual degraded model cards

- Simulation 2
  - Fresh vs. Aged Simulation

- Reliab. test structures
- Static stress
  - $I_{sub}$, lifetime and AGEMOS model parameters
RelXpert Netlist Example

title DC verification for Ids-vds|vgs
.include 'model/nmos.pm3'
.options brief=0 post

* Relxpert statments
*Relxpert:.age 10min
*Relxpert: .deltad 0.1
*Relxpert:.agemethod agemos

* normal operating condition
vds 1 0  3.3
vgs 2 0  1.5
vb 4 0 0.0
m1 1 2 0 4 nch3 l=0.35u w=10u
vids 3 1 0
.print tr i1(m1)
.tran 1n 10n
.end

.model  nch3  nmos level = 49
+vth0 = 0.735  k1 = 1.0141647
...

***************************************************************
*               RelXpert Isub-Igate model parameters
***************************************************************
+ai = 4.0933e+007  ecrit0 = 9936.5       ecritg = 17846
***************************************************************
*               RelXpert Life Time model parameters
***************************************************************
+h0 = 2.1152e+005  m0 = 3.423  nn0 = 0.48174
+mgd = 0            nbemod = 2
***************************************************************
*               RelXpert AgeMos model parameters
***************************************************************
+hd1_vth0= 8.85      hd2_vth0= 13     hn1_vth0= 0.67
+hs_vth0 = 2.6       hd1_u0  = 9.4       hd2_u0  = 1.5
+hn2_u0  = 0          hs_u0  = 0.82381   hd1_vsat= 4.25
+hn1_vsat= 0.529     hn2_vsat= 1        hs_vsat = 1

Model parameters:

These are the same model-card parameters that are statistically varied for local mismatch analysis!

Effect of Process Drift or Degradation on Yield (M. Pronath)

An open question: How do the statistical parameters of the model change with/by aging?

Determine the yield in 10 years?

MunEDA User Group Meeting: Challenges in Analog/Mixed-Signal EDA

9/15/2007
Vision:
A hierarchical A/MS DfY/DfM Design- and Analysis-Flow

Tools
Analog Insydes
WiCkeD
RelXpert

Challenges
- Hierarchy
- Multi-domain modeling
Motivation for Behavioral Modeling

- Simulation on transistor level?
  - very long simulation times
  - often very complex circuits
  - simulation of heterogeneous systems (overall) not possible

- Hierarchical simulation and sizing
  → Helmut Gräb

- Hierarchical design centering ("SABM" - statistical ABM)?

Design Methods Incorporating Behavioral Modeling
Model Taking into Account Self-Heating (IFX)

Extension of model by a thermal network

Thanks to K.-W. Pieper
Problem Transformation to Mechatronic Systems

<table>
<thead>
<tr>
<th>analogies</th>
<th>electronics</th>
<th>mechanics</th>
</tr>
</thead>
<tbody>
<tr>
<td>through variables</td>
<td>current</td>
<td>force, torque</td>
</tr>
<tr>
<td>across variables</td>
<td>voltage</td>
<td>displacement, rotation</td>
</tr>
<tr>
<td>equation setup</td>
<td>Kirchhoff laws</td>
<td>d’Alembert’s principle</td>
</tr>
</tbody>
</table>

- Decompose mechanical system in finite elements
- Implement elements in terms of (symbolic) component models

Bridging to Mechatronic – Modeling and Simulation of Mechatronic Systems by Circuit Models

- FEM-simulation
- System simulation with network/circuit models
  - basic block
  - complex geometries
  - Full system simulation under inclusion of mechanical and electrical excitation

idea by FhG IIS/EAS, Dr. P. Schwarz
Bridging to Mechatronic –
Modeling with equivalent networks: Analytical models (FhG IIS/EAS)

Library with basic models for micro-system applications
(MEMS - Micro-Electro-Mechanical Systems):

<table>
<thead>
<tr>
<th>Library</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANCHOR2D</td>
<td>Anchor</td>
</tr>
<tr>
<td>BEAM2DE</td>
<td>Linear beam</td>
</tr>
<tr>
<td>COMB2D</td>
<td>Comb-structure</td>
</tr>
<tr>
<td>F2D</td>
<td>External Force</td>
</tr>
<tr>
<td>GAP2D</td>
<td>Parallel beam with electrostatic force</td>
</tr>
<tr>
<td>GAP2DE</td>
<td>Parallel beam with electrostatic force and electrical resistance</td>
</tr>
<tr>
<td>DAMPING</td>
<td>Damping-element</td>
</tr>
<tr>
<td>MASS</td>
<td>Mass</td>
</tr>
<tr>
<td>SPRING</td>
<td>Spring</td>
</tr>
</tbody>
</table>

Behavioral model for a homogeneous beam segment

Multi-Physical Modeling – More Analogies
Classes Based on Energy Flow (Modelica)

<table>
<thead>
<tr>
<th>Domain Type</th>
<th>Potential</th>
<th>Flow</th>
<th>Carrier</th>
<th>Modelica Library</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td>Voltage</td>
<td>Current</td>
<td>Charge</td>
<td>Electrical. Analog</td>
</tr>
<tr>
<td>Translational</td>
<td>Position</td>
<td>Force</td>
<td>Linear momentum</td>
<td>Mechanical. Translational</td>
</tr>
<tr>
<td>Rotational</td>
<td>Angle</td>
<td>Torque</td>
<td>Angular momentum</td>
<td>Mechanical. Rotational</td>
</tr>
<tr>
<td>Magnetic</td>
<td>Magnetic potential</td>
<td>Magnetic flux rate</td>
<td>Magnetic flux</td>
<td></td>
</tr>
<tr>
<td>Hydraulic</td>
<td>Pressure</td>
<td>Volume flow</td>
<td>Volume</td>
<td>HyLibLight</td>
</tr>
<tr>
<td>Heat</td>
<td>Temperature</td>
<td>Heat flow</td>
<td>Heat</td>
<td>HeatFlow1D</td>
</tr>
<tr>
<td>Chemical</td>
<td>Chemical potential</td>
<td>Particle flow</td>
<td>Particles</td>
<td>Under construction</td>
</tr>
<tr>
<td>Pneumatic</td>
<td>Pressure</td>
<td>Mass flow</td>
<td>Air</td>
<td>PneuLibLight</td>
</tr>
</tbody>
</table>
Another Example of Problem Transformation:
Magnetic Circuits → Electrical Networks

- Small example of magnetic circuit

Multi-Physical Systems –
Benefits of Common Modeling Approach

- Increase understanding of complex systems
- Design and optimization
- Virtual prototyping
- Verification

Build more complex systems
Topics for Innovation Activities in EDA

- Design for Yield (DFY)
  - Strategies and algorithms for high yields ("6σ-designs")
  - Advanced sampling strategies
  - Design space exploration
  - Statistical static timing analysis (SSTA)
- Hierarchical circuit simulation, optimization and design centering
- Advanced circuit/system analysis and circuit/system modeling
  - Application of symbolic techniques (& combination with numerical methods)
  - Automated behavioral modeling
  - Modeling strategy for analog/mixed-signal blocks (including hierarchy)
  - Inclusion of statistics in behavioral models to allow for hierarchical design centering
  - Multi-physical systems: Modeling, simulation optimization & design centering
  - Inclusion of aging and reliability
- Top-down design methodology
  - Reuse (topology, combination and embedding of blocks, design information)
  - Design-space exploration
  - Constraint management
  - Verification cockpit
Outlook:
Design Abstraction Levels – Challenges for DfY & DfR

DfY methodology and tools – future challenge

Digital → SSTA and Analog/Mixed-Signal ("SABM")

DfY methodology and tools available today
WiCkeD Circuit Optimization Examples:

- Optimization and Centering of the Basic Cells of SRAM Memories
- Performance & Yield Optimiz. of Sense Amp for Automotive Applications

Elena Raciti
Application Engineer NVM Analog/Mixed-Signal Flows
elena.raciti@st.com

STMicroelectronics
www.st.com

About STMicroelectronics
STMicroelectronics is one of the world’s largest semiconductor companies with net revenues of US$9.85 billion in 2006 and US$4.69 billion for the first half of 2007.

The Company’s sales are well balanced between the semiconductor industry’s five major high-growth sectors (percentage of ST’s sales in 2007): Communications (35%), Consumer (17%), Computer (16%), Automotive (16%) and Industrial (16%).

According to the latest industry data, ST is the world’s fifth largest semiconductor company with market leadership in many fields. For example, ST is the leading producer of application-specific analog chips and power conversion devices. It is also the #1 supplier of semiconductors for the Industrial market and for set-top box applications, and occupies leading positions in fields as varied as discrete devices, camera modules for mobile phones and automotive integrated circuits.
WiCkeD Circuit Optimization Examples:
A) Optimization & Centering of the Basic Cells of SRAM Memories
B) Performance & Yield Optimization of a Sense Amplifier for Automotive Applications

Elena Raciti
Application Engineer
NVM Analog/Mixed-Signal Flows
FTM – Central CAD & Design Solutions
STMicroelectronics, Agrate – Italy
Outline

- Context: overview on design flow architecture & integration of statistical sizing methods in STMicroelectronics
  - presented in detail yesterday by Pierluigi Daglio

- Example #1 → optimization of the leakage current of an SRAM (technology: CMOS 90nm)

- Example #2 → analysis and optimization of a sense amplifier (technology: CMOS 90nm)

Conclusions

Context: WiCkeD design flow
Example 1: SRAM optimization

**TARGET:** improve the leakage current of a SRAM core (CMOS 90nm) keeping, at the same time, good values for all other performances

**TESTBENCH:**
- Core made of 4096 basic cells: 512 rows x 8 column
- Voltage sources \( V_n \) for the computation of static noise margin
- Input stimuli: WL – word line, BL – true bit line, BLB – false bit line

**Example 1: SRAM optimization**

**TARGET:** improve the leakage current of a SRAM core (CMOS 90nm) keeping, at the same time, good values for all other performances

**TESTBENCH:**
- Core made of 4096 basic cells: 512 rows x 8 column
- Voltage sources \( V_n \) for the computation of static noise margin
- Input stimuli: WL – word line, BL – true bit line, BLB – false bit line

---

**Testbench**

**Input stimuli & performances in Eldo syntax:**

<table>
<thead>
<tr>
<th>Stimuli</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{power} ) = 0 Vp</td>
<td>( I_{leak} )</td>
</tr>
<tr>
<td>( V_{wl1} ) = 0 DC 0 PWL 0 0 1.49u 0 1.50u Vp 103u Vp 103.1u 0</td>
<td>( I_{off} )</td>
</tr>
<tr>
<td>( V_{wl2} ) = 0 DC 0 PULSE(0 Vp 105u 0.1n 0.1n 1n 2.5n)</td>
<td>( I_{on} )</td>
</tr>
<tr>
<td>( V_{bit} ) = 0 DC Vp PWL 0 Vp 103.2u Vp 120u 0</td>
<td>( \text{SNM}_r )</td>
</tr>
<tr>
<td>( V_{bitb} ) = Vp</td>
<td>( \text{WM} )</td>
</tr>
</tbody>
</table>

**PERFORMANCES**

- \( \text{extract DC label} = I_{leak} \ abs((V_{power})/4096) \)
- \( \text{extract TRAN label} = I_{off} \ abs(valat(i(XI0.XM5.M1.d),at=1.25u)) \)
- \( \text{extract TRAN label} = I_{on} \ abs(valat((i(XI0.XM5.M1.d),at=1.75u)) \)
- \( \text{extract TRAN label} = \text{ratio} \ (\text{extract}(I_{on})/\text{extract}(I_{off})) \)
- \( \text{extract TRAN label} = \text{SNM}_r \)
- \( \text{extract TRAN label} = \text{WM} \)
- \( \text{extract DC label} = \text{Delta}_vdd \ v(VDD!,virtual_vdd) \)
- \( \text{extract DC label} = \text{Delta}_gnd \ v(virtual_gnd,0) \)
Circuit settings (1)

Definition of the performances and their specifications:

<table>
<thead>
<tr>
<th>Performance</th>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_leak</td>
<td>Leakage current</td>
<td>&lt; 150 pA</td>
</tr>
<tr>
<td>WM</td>
<td>Write margin</td>
<td>&gt; 100 mV</td>
</tr>
<tr>
<td>SNM_r</td>
<td>Static noise margin (in read phase)</td>
<td>&gt; 100 mV</td>
</tr>
<tr>
<td>Ratio</td>
<td>Ratio between READ current (Ion) &amp; off current (Ioff)</td>
<td>&gt; 7000</td>
</tr>
<tr>
<td>Delta_VDD</td>
<td>Difference between VDD and virtual_VDD</td>
<td>&lt; 310 mV</td>
</tr>
<tr>
<td>Delta_GND</td>
<td>Difference between virtual_GND and GND</td>
<td>&lt; 610 mV</td>
</tr>
</tbody>
</table>

Circuit settings (2)

Parameters:

- Process parameters: all the ones defined into the libraries (both LOT and DEV)
Circuit analysis

Results of the Worst Operating Analysis

<table>
<thead>
<tr>
<th>Performance</th>
<th>Specification Type</th>
<th>Lower Worst-Case</th>
<th>Upper Worst-Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delta_gnd</td>
<td>Upper</td>
<td>-40 1.32</td>
<td>594.7 m</td>
</tr>
<tr>
<td>Delta_vdd</td>
<td>Upper</td>
<td>-40 1.32</td>
<td>293.2 m</td>
</tr>
<tr>
<td>I_leak</td>
<td>Upper</td>
<td>150 1.32</td>
<td>45.05 p</td>
</tr>
<tr>
<td>SNM</td>
<td>Lower</td>
<td>150 900 m</td>
<td>177.5 m</td>
</tr>
<tr>
<td>VM</td>
<td>Lower</td>
<td>-40 900 m</td>
<td>223.1 m</td>
</tr>
<tr>
<td>ratio</td>
<td>Lower</td>
<td>150 900 m</td>
<td>28.42 k</td>
</tr>
</tbody>
</table>

All the specifications are fulfilled also in front of variations of the operating parameters

Circuit optimization

Step 1 – Feasibility Optimization
- No constraint → no Feasibility Optimization needed

Step 2 – Nominal Optimization
- All the specification are fulfilled also in front of variations of operating parameters → no Nominal Optimization needed

Step 3 – Yield Optimization
- Results of the Worst Case Analysis:

<table>
<thead>
<tr>
<th>Performance</th>
<th>Specification</th>
<th>Analysis</th>
<th>Worst-Case Distance</th>
<th>Yield %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delta_gnd</td>
<td>&lt; 610 m</td>
<td></td>
<td>8.332</td>
<td>02.404</td>
</tr>
<tr>
<td>Delta_vdd</td>
<td>&lt; 310 m</td>
<td></td>
<td>1.377</td>
<td>91.563</td>
</tr>
<tr>
<td>I_leak</td>
<td>&lt; 150 p</td>
<td></td>
<td>4.412</td>
<td>93.950</td>
</tr>
<tr>
<td>SNM</td>
<td>&gt; 100 m</td>
<td></td>
<td>5.192</td>
<td>100.000</td>
</tr>
<tr>
<td>VM</td>
<td>&gt; 100 m</td>
<td></td>
<td>4.824</td>
<td>100.000</td>
</tr>
<tr>
<td>ratio</td>
<td>&gt; 7 k</td>
<td></td>
<td>3.216</td>
<td>99.935</td>
</tr>
</tbody>
</table>

Yield optimization needed
Yield optimization results (1)

- WiCkeD Monte Carlo Analysis results:
  - Operating conditions set to worst case
  - Number of simulations: 1000 for each performance

<table>
<thead>
<tr>
<th>Performance</th>
<th>Operating conditions</th>
<th>Worst value</th>
<th>Mean value</th>
<th>σ</th>
<th>Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_leak</td>
<td>150°C;1.32V</td>
<td>132 pA</td>
<td>53 pA</td>
<td>14 pA</td>
<td>100%</td>
</tr>
<tr>
<td>SNM_r</td>
<td>150°C;0.9V</td>
<td>124 mV</td>
<td>170 mV</td>
<td>15 mV</td>
<td>100%</td>
</tr>
<tr>
<td>WM</td>
<td>-40°C;0.9V</td>
<td>160 mV</td>
<td>235 mV</td>
<td>25 mV</td>
<td>100%</td>
</tr>
<tr>
<td>Ratio</td>
<td>150°C;0.9V</td>
<td>9170</td>
<td>28300</td>
<td>11000</td>
<td>100%</td>
</tr>
<tr>
<td>Delta_VDD</td>
<td>-40°C;1.32V</td>
<td>312 mV</td>
<td>268 mV</td>
<td>13 mV</td>
<td>99.9%</td>
</tr>
<tr>
<td>Delta_GND</td>
<td>-40°C;1.32V</td>
<td>603 mV</td>
<td>538 mV</td>
<td>21 mV</td>
<td>100%</td>
</tr>
</tbody>
</table>

- Delta_VDD limits the yield value
- The final cell has a smaller area (~19%) than the initial one

Yield optimization results (2)

- How WiCkeD worked
  - Delta_vdd distributions, before & after the optimization:

- Standard deviation is equal but mean value has been decreased
- Performances with a good initial yield have been worsened, like SNM and WM
Example 2: Sense Amplifier analysis & optimization

**TARGET:**
- Analyze in which conditions a sense amplifier doesn't work
- Make it robust to the variations of both process and operating parameters

**TESTBENCH:**
- $mbls$ is compared with an internal reference node ($gain_{ref}$)
- $s_{out}$ is the digital output
- $R_{19}$ is a fictitious resistor that represents the current through the flash memory cell
- Two instances for the two analysis: .TRAN and .AC

Circuit settings (1)

Definition of the performances:

<table>
<thead>
<tr>
<th>Performance</th>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase_margin</td>
<td>phase margin of the node $mbls$</td>
<td>&gt;45º</td>
</tr>
<tr>
<td>$V_{diff}$</td>
<td>voltage difference between $mbls$ and the reference node $gain_{ref}$</td>
<td>&gt; 100 mV</td>
</tr>
</tbody>
</table>

In Eldo syntax:

```eldoscript
*** PHASE MARGIN ***
defmac phmarg(a,b) = 180 - abs(xycond(a, b<=0.0) - yval(a, 1))
.extract AC label = phase_margin $phmarg(vp(XI0.mbls_ac), vdb(XI0.mbls_ac))

*** DIFFERENCE VOLTAGE GAIN_REF - MBLS ***
defwave diff = abs(v(XI0.gain_ref_tran)-v(XI0.mbls_tran))
.extract TRAN label = v_diff valat(w(diff), at=68n)
```
Circuit settings (2)

- Constraints: critic transistors in saturation
  - NMOS:
    - Saturation → \( V_{ds} - (V_{gs} - V_{th}) - 0.01 \geq 0 \)
    - Strong inversion → \( (V_{gs} - V_{th}) - 0.1 \geq 0 \)
  - PMOS:
    - Saturation → \( -V_{ds} + (V_{gs} - V_{th}) - 0.01 \geq 0 \)
    - Strong inversion → \( -(V_{gs} - V_{th}) - 0.1 \geq 0 \)

- Parameters:
  - Design
    - \( W \) & \( L \) of the “analog” transistors
    - Ranges of variation: ±20%
  - Process
    - All the LOT parameters
    - The DEV parameters related to the “analog” transistors
  - Operating
    - Temperature and \( V_{dd} \)

Circuit analysis (1)

- Ranges for operating parameters:
  - \( R_{19} \) fixed to 60kΩ
  - Results of Worst Case Operating Analysis:

<table>
<thead>
<tr>
<th></th>
<th>Min. value</th>
<th>Typ. value</th>
<th>Max. value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp</td>
<td>-40°C</td>
<td>25°C</td>
<td>150°C</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.08V</td>
<td>1.2V</td>
<td>1.32V</td>
</tr>
</tbody>
</table>

Nominal Optimization needed
## Circuit analysis (2)

Values of the constraint in typical operating conditions

<table>
<thead>
<tr>
<th>Performances</th>
<th>Constraints</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase_margin</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_diff</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table:**

- **NMOS**:
  - Phase_margin: ~11.03 m
  - V_diff: ~76.77 m

- **PMOS**:
  - Phase_margin: ~11.03 m
  - V_diff: ~76.77 m

### Feasibility

Optimization needed

---

## Circuit analysis (3)

**Results from the initial WiCkED Monte Carlo Analysis:**

- 3000 samples for each performance
- Operating conditions fixed to worst case

**Graphs:**

- **Phase_margin**
  - Mean Value: 62.034
  - Min. Value: 62.006
  - Max. Value: 62.061
  - Standard Deviation: 0.2374
  - Variance: 0.0562

- **V_diff**
  - Mean Value: 315.81
  - Min. Value: 124.74
  - Max. Value: 315.81
  - Standard Deviation: 12.9959
  - Variance: 169.996

**Total initial yield** = ~3%
Optimization results

After Feasibility and Nominal Optimization:

<table>
<thead>
<tr>
<th>Performance</th>
<th>Lower Value</th>
<th>Value</th>
<th>Upper Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>phase_margin</td>
<td>52.96</td>
<td>56.07</td>
<td>45</td>
</tr>
<tr>
<td>v_diff</td>
<td>102.4 m</td>
<td>240.74 m</td>
<td>100 m</td>
</tr>
</tbody>
</table>

After Yield Optimization:

<table>
<thead>
<tr>
<th>Performance</th>
<th>Performance Value</th>
<th>Specification</th>
<th>Worst Case Distance</th>
<th>Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>phase_margin (lower)</td>
<td>62.962</td>
<td>45</td>
<td>5.429</td>
<td>100.000</td>
</tr>
<tr>
<td>v_diff (lower)</td>
<td>326.7 m</td>
<td>100 m</td>
<td>6.543</td>
<td>100.000</td>
</tr>
</tbody>
</table>

Final results

Validation of the obtained results through a MCA:
- 3000 samples for each performance
- Operating conditions fixed to worst case

Both the performances now fulfill their specifications
Circuit analysis (1)

- Further deeper analysis in order to:
  - Determine the range of values of R_{19} in which the amplifier doesn’t work (V\_diff \approx 0V)
  - Find the minimum value of R_{19} that guarantees V\_diff > 100mV in front of variations of ALL the parameters
  - Considered range of variation for R_{19}: 60k\Omega \div 750k\Omega
  - Results from a parameter sweep of R_{19}:

![Graph showing V\_diff VS R_{19}](image)

\( 88k\Omega \)

Circuit analysis (2)

- Followed procedure (alternative to a series of MCA):
  1. In the worst case operating conditions for V\_diff (temp=150°C, Vdd=1.32V), determine which is the starting point in the range of R_{19}
  2. Use the Worst Case Analysis in order to find the minimum value that gives a partial yield equal 100%
  3. Validate the exact minimum value through a Monte Carlo Analysis

**STEP 1**: The minimum value that makes V\_diff to be >100mV is 145k\Omega

![Graph showing V\_diff VS R_{19}](image)

\( 145k\Omega \)
Circuit analysis (3)

STEP 2: Worst Case Analysis repeated for values larger than 145kΩ of R₁₉ gives a yield of 100% for R₁₉=200kΩ

<table>
<thead>
<tr>
<th>Performance</th>
<th>Specification</th>
<th>Analysis</th>
<th>Worst-Case Distance</th>
<th>Yield [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_diff</td>
<td>&gt; 100 m</td>
<td></td>
<td>4.500</td>
<td>100.000</td>
</tr>
</tbody>
</table>

STEP 3: Monte Carlo Analysis proved that the minimum value for R₁₉ that guarantees a yield of 100% is 220kΩ

Conclusions

Two examples of the analysis and optimization using WiCkeD of two critical analog designs in STM has been presented

SRAM:
- the starting point was already a good point and a fine tuning was necessary

Sense amplifier:
- the starting point was not good so all the optimization steps were needed in order to obtain a well working circuit
- Using the features available in WiCkeD it has been possible to deeply analyze the circuit in the least amount of time
Qualification of WiCkeD for the austriamicrosystems DFM-DFY design flow

About austriamicrosystems
austriamicrosystems is a global leader in the design and manufacture of high performance analog ICs (integrated circuits). We develop and produce industry-leading customized and standard analog semiconductors, these include customized ASICs (Application Specific Integrated Circuits) and high performance standard product solutions.

austriamicrosystems focuses on the areas of power management, sensors & sensor interfaces, portable audio and car access in its markets Communications, Industry & Medical and Automotive, complemented by its Full Service Foundry activities. We combine more than 25 years of analog design capabilities and system know-how with our own state-of-the-art manufacturing and test facilities, offering the benefits of a vertically integrated full-service supplier.

austriamicrosystems leverages its significant expertise in low power consumption and high accuracy to provide highly integrated best-in-class products for communications, industrial, medical technology and automotive markets worldwide. We bring our world-class capabilities to exciting products for power management, MP3 players, MEMS microphones, diabetic blood glucose measurement, automotive safety systems such as ESP, solid state electricity meters, sensor interfaces and many other applications. Many of our customers are well-known brands and rely on austriamicrosystems as their sole source supplier of choice.

Thomas Mörth
Section Manager Design Support
thomas.moerth@austriamicrosystems.com

austriamicrosystems AG
www.austriamicrosystems.com
Qualification of WiCkeD for the austriamicrosystems DFM-DFY design flow

MUNEDA User Group Meeting
Thomas Mörth
26. September 2007

Overview

– Company Introduction
– austriamicrosystems DFM/DFY Design Flow
– Wicked Integration
– Summary
Overview

- Company Introduction
- austriamicrosystems DFM/DFY Design Flow
- Wicked Integration
- Summary
Analog DFM Flow - Overview

- **Pre-Layout**:
  - Schematic Entry
  - Pre-Layout Simulation (estimated parasitics)
  - WiCkeD

- **Layout & Verification**:
  - Layout Entry
  - Layout Verification

- **Post-Layout**:
  - Parasitic Extraction
  - Post-Layout Simulation (extracted parasitics)
  - WiCkeD
  - Finish Layout & tape out

---

Analog DFM Flow - Pre Layout

- **Virtuoso Schematic Editor**
  - Design Architect IC, ICC

- **Pre-Layout Simulation (estimated parasitics)**
  - Spectre, AMS-Designer
  - Eldo, Advanced MS

- **ESD-Checker**

- **Nominal Design**

- **Worst Case**

- **Yield Analysis**
  - Yield Optimisation
  - WiCkeD

- **HK Library cells**
  - Foundry IP
  - Special IP

- **Parasitic Models**
  - SOAC Models
  - Corner Models
  - Monte Carlo M.
Analog DFM Flow - Layout Verification

Pre-Layout Simulation

Virtuoso XL, VCR, CCAR
IC Station

Layout Entry

DRC
LVS
Leak Check
ESD Check
Latch up Check

Parasitic Extraction

Assura
Calibre

Run sets

Pcells

Library Cells

IP Cells

Generators

Analog DFM Flow - Post Layout

Schematic Entry

Layout Entry

Parasitic Extraction

Assura RCX
Calibre XRC

Post-Layout Simulation
(extracted parasitics)

Nominal Design
Worst Case

WiCkeD

Yield Analysis
Yield Optimisation

Finish Layout & tape out

Non-Parasitic Models

SOAC Models
Corner Models
Monte Carlo M.
Overview

- Company Introduction
- austriamicrosystems DFM/DFY Design Flow
- Wicked Integration
- Summary

Wicked Integration

What was needed to be done?

- Callbacks
- Simulation Models
- Technology Setup
- Server Farm Integration
Callbacks

- Callbacks are needed by the design flow
- Initial software was not able to execute callbacks during optimisation
- Prove of concept implementation delivered by Muneda
  ➔ Need to be implemented in next official Wicked version!

- Verification of correct callback execution

Simulation Models

- Monte Carlo models needed update
- Parameters for Vth mismatch and U0 mismatch had to be added.
- Generator script had to be adopted
- Model verification environment had to be adopted
Technology Setup

Creation of the ceconfiguration.xml

- Which parameters of the devices should be used for optimisation?
- Which parameters are calculated by the callback
- Verification of callbacks
- Creation of the file automated with model file generation

Server Farm Integration

- 100+ CPUs (Ultra Sparc & Opteron)
- Running batch & interactive jobs for design and test departments
- Dedicated CPUs for Wicked not possible
- Sim Server are local
- Simulation Jobs are distributed
Server Farm Integration – Problems & Solutions

P  Simulation license checkout problems were not shown in Wicked report window

S  start_spectre script corrected to populate the error from simulator. License queuing enabled to prevent “no license” problem.

P  Sim Server died after some time.

S  Seemed to be related to Linux Kernel. Solution was to set LD_ASSUME_KERNEL to 2.4.1

P  Initial Setup:  Sim Server local.
     Simulation job distributed.
     Post processing local.
     This setup showed problems under high load. Synchronization between simulation job and post processing job did not always work.

S  Final setup:  Sim Server local.
     Simulation & post processing distributed as one job.

Overview

– Company Introduction
– austriamicrosystems DFM/DFY Design Flow
– Wicked Integration
– Summary
Conclusion

- austriamicrosystems integrated Wicked into the internal DFM/DFY design flow
- Major problems were Server Farm integration and callback implementation
- Technical help from Muneda was excellent
- austriamicrosystems “adoptions“ of Wicked still need to be released in an official version.

Thank you for your attention
Technology Setup for WiCkeD in X-FAB CMOS and BiCMOS Process for Automotive and Sensor Applications

Dr. Volker Boos
volker.boos@erfurt.imms.de

Hagen Wald
hagen.wald@xfab.com

IMMS gGmbH
www.imms.de

X-Fab Semiconductor Foundries AG
www.xfab.com

About IMMS
Institute for Microelectronic and Mechatronic Systems is a non-profit Research and Development organisation based in Ilmenau and Erfurt, Germany. It was set up to offer industry practical product development with a sound academic foundation, thus assisting in getting technological innovations onto the market. The main Research and Development activity at IMMS is the creation of complex engineering systems, largely involving heterogeneous microelectronic and mechanical components.

About X-Fab
As the world's leading foundry group for mixed-signal semiconductor applications, X-FAB creates a clear alternative to typical foundry services by combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service, a high level of responsiveness and first-class technical support. These key elements allow X-FAB to optimally manage the flow of product development and the supply chain for its customers' semiconductor products.
Setup WiCkeD for X-FAB Processes

Dr.-Ing. Volker Boos (IMMS)
Dr. Hagen Wald (X-FAB)

The Erfurt Microelectronics Site

X-FAB
Haarbergstr. 67
99097 Erfurt

IMMS gGmbH
Konrad-Zuse-Straße 14
99099 Erfurt

Erfurt-South-East - Centre of the Microelectronics of Thuringia
X-FAB · Melexis · CIS · IMMS · and others
X-FAB Process Overview

X-FAB mixed-signal process technologies supported by IMMS WiCkeD setups:

<table>
<thead>
<tr>
<th>Technology</th>
<th>Struct. Size (μm)</th>
<th>Type</th>
<th>Statistics</th>
<th>Application area</th>
</tr>
</thead>
<tbody>
<tr>
<td>XB06</td>
<td>0.6</td>
<td>Bi-CMOS</td>
<td>Yes</td>
<td>Optoelectronic, Sensors, integrated photodiodes</td>
</tr>
<tr>
<td>XC06</td>
<td>0.6</td>
<td>CMOS</td>
<td>No</td>
<td>RF-Circuits</td>
</tr>
<tr>
<td>XC035</td>
<td>0.35</td>
<td>CMOS</td>
<td>Yes</td>
<td>No more supported, use xh035</td>
</tr>
<tr>
<td>XB035</td>
<td>0.35</td>
<td>Bi-CMOS</td>
<td>No</td>
<td>Currently not supported</td>
</tr>
<tr>
<td>XH035</td>
<td>0.35</td>
<td>CMOS</td>
<td>Yes</td>
<td>Sensor amplifier, RF circuits</td>
</tr>
<tr>
<td>XI10</td>
<td>1.0</td>
<td>SOI</td>
<td>Yes</td>
<td>Automotive, high temperature applications</td>
</tr>
<tr>
<td>XC018</td>
<td>0.18</td>
<td>CMOS</td>
<td></td>
<td>Design kit not yet integrated into WiCkeD</td>
</tr>
</tbody>
</table>

See [www.xfab.com](http://www.xfab.com) for more details

---

XB06 Process

- 0.6μ Mixed-Signal BiCMOS
- High precision analog and RF applications mixed with digital parts for telecommunication, consumer, automotive and industrial products
- Fast npn bipolar transistors
- Integrated optical devices
- Integrated RF devices
**XI10 Process**

- Dielectric isolated mixed-signal (multi-voltage systems)
- High temperature (up to 225°C)
- High voltage (up to 130V breakdown voltage)
- Intrinsic radiation hardness
- 42 V automotive board net

**XH035 Process**

- 0.35-micron Modular RF capable Mixed Signal Technology
- Applications
  - High precision, low-power mixed-signal circuits
  - Analog front ends for sensors
  - RF Applications
  - Communications, consumer, automotive and industrial markets
- Modular concept
  - Low threshold voltage option
  - Low leakage process option
  - 5V dual gate or 5V only module
  - Capacitors with high capacitance area
  - High voltage devices (14V, 18V and 45V)
  - 10KΩ/ extra high resistive poly
  - Well isolated 3.3V and 5V devices
XC018 Process

- New fab in Malaysia
- First release of design kits available
- IMMS will create WiCkeD setup files
- XC018 : Modular 0.18 µm CMOS process
- XH018 will support 32 V (planned)

X-FAB Design Kits

- Simulators supported : Spectre, HSpice and ELDO
- Spectre file structure
  - Top-level file <processname>.scs
  - Subdirectories for models
- Basic kit contains sections for corner simulations
  - tm : typical mean - wo : worst one
  - wp : worst power - wz : worst zero
  - ws : worst speed
- Statistics not in all kits
  - as section mc_g (XB06)
- Sample
  - xb06.scs

```plaintext
library xb06
section tm
include "$T_DIR/spectre/xb06/models/bsim3v3/tm/<modname>.scs"
...
endsection tm
section wp
include "$T_DIR/spectre/xb06/models/bsim3v3/wp/<modname>.scs"
...
```
X-FAB Models in Design Kit

- Transistors defined as subcircuits

```verbatim
simulator lang=spectre
subckt modn (d g s b)
parameters w=1e-6 l=1e-6 ad=0 as=0 pd=0 ps=0 nrd=0 nrs=0
ml (d g s b) modnmod w=v l=1 ad=ad as=as pd=pd ps=ps nrd=nrd nrs=nrs
model modnmod bsim3v3 version=3.10 type=n
+ ... 
ends modn
```

- Device names not equal to model names
  - Extract from ceconfiguration.xml for XB06:

```xml
<NMOSTRANSISTORS>
  <ENTITYDEVICE LIB="PRIMLIB" CELL="nmos4"/>
  ...
  <MODELS SIMULATORTYPE="SPECTRE">
    <ENTITYMODEL IDENTIFIER="modn" DESCRIPTION="n-mos transistor"
      TYPE="TRANSISTOR">
      <HIERARCHY DEVICEPATH=".m1"/>
  ...
```

Statistics in XB06 and XH035 Design Kits

- Section mc_g (Monte Carlo Models – Gaussian) in top-level file

```verbatim
section mc_g
include "$T_DIR/spectre/xb06/mc_params/spectre_gauss.scs"
include "$T_DIR/spectre/xb06/models/bsim3v3/mc/<modname>.scs"
...
```

- Parameters sorted by model (Values x-ed for confidence)

```verbatim
simulator lang=spectre
parameters
  // modn:
  + vtmn = x.x20e-01
  + cgado = x.x00e-10
  + tgox = x.x00e-08
  ...
statistics{
  process{
    // modn:
    vary vtmn dist=gauss std=x.x00e-02
    vary cgado dist=gauss std=x.x00e-11
    vary tgox dist=gauss std=x.x00e-10
    ...
```
Statistics in the Models

- **Mismatch parameters (spectre_gauss.scs, cont.)**

  ```plaintext
  } End of process section
  mismatch{
  vary Avt_modn  dist=gauss  std=x.x00e-02
  vary AU0_modn  dist=gauss  std=x.x00e-03
  ...
  ```

- **Model file (modn.scs in XB06)**

  ```plaintext
  simulator lang=spectre
  subckt modn (d g s b)
  parameters w=1e-6 l=1e-6 ad=0 as=0 pd=0 ps=0 nrd=0 nrs=0
  ml (d g s b) modnmod w=w l=l ad=ad as=as pd=pd ps=ps nrd=nrd nrs=nrs
  model modnmod bsim3v3 version=3.10 type=n
  + ...
  + vth0=(vtmn+(Avt_modn/sqrt(1e+12*(w+(0.000e+00))*(l+(-3.500e-07)))))
  + ...
  + u0=(u0n*(1+AU0_modn/sqrt(1e+12*(w+(0.000e+00))*(l+(-1.000e-07))))))
  ```

Integration of WiCkeD into the IMMS Design Flow

- **Setup files structure**
  - IMMS wide files in /progs/init/wicked/
  - One subdirectory per technology
  - User files in $HOME if needed
  - Own functions integrated
    - Function „myphasemargin“ in functions.ocn

- **Entries in the Cadence startup script**

  ```plaintext
  setenv WICKED_CONFIG_PATH "/progs/init/wicked/$1[:~/wicked]"
  setenv WICKED_DP_MODE RSH
  ```

- **Entries in .cdsinit_personal**

  ```plaintext
  load("/progs/muneda/wicked/current/interface/config/WiCkeD.il")
  ```
Sample in Bi-CMOS

- The investigated circuit has a P-MOS differential amplifier having resistors as input. The output stage is a push-pull amplifier with NPN transistors only, because the output voltage has to be smaller than 1 V. An op-amp controls the output stage.

- The simulation results are insufficient:
  - low gain
  - low slew rate
  - stability problems

Sample in Bi-CMOS - optimized

- Nominal optimization with WiCkeD leads to slight improvements only

- Critical points analyzed
  - with sensitivity analysis

- Topological changes
  - input stage with active load
  - additional stage with phase correction
  - better push-pull output stage
Optimization Results of Output Opamp

<table>
<thead>
<tr>
<th>CL=20pF</th>
<th>Starting solution</th>
<th>Optimized Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain A0 (dB)</td>
<td>37</td>
<td>73</td>
</tr>
<tr>
<td>SlewRate (rise/fall V/μs)</td>
<td>920 / 480</td>
<td>660 / 820</td>
</tr>
<tr>
<td>Phase margin (degrees)</td>
<td>41</td>
<td>53</td>
</tr>
<tr>
<td>Power (mA)</td>
<td>3.44</td>
<td>3.6</td>
</tr>
<tr>
<td>Transient signal</td>
<td>overlaid with oscillations</td>
<td>clean signal</td>
</tr>
</tbody>
</table>

Sample in SOI: Power supply for 42 V

- Testbench for controlling op-amp
- Import into WiCkeD
- Feasible solution
- Only small improvements by nominal optimization
- Reasons detected by nominal analysis
- Topological changes
- Optimizing PSRR
Optimizing SOI Power Supply

- Results of optimization (PSRR improvement) published on EUROSOI 2005 in Granada

This transistor has most influence to PSRR

Sample in XH035

- Topology & initial solution
  - Topological changes to ensure DC operating point of the output stage
  - No acceptable feasible solution found for all Ls and Ws set to minimal values. Setting some parameters manually
  - Setting factor for non-symmetrical current mirror to 1.5

- Constraints
  - Two level shifter at the cascode transistors deleted.

- Optimizing
  - With good initial feasible solution, the optimization returns with a good result.
MEDEA+ Project HONEY

- Highly Optimized Design Methods for Yield and Reliability
- HONEY will propose a yield- and reliability-oriented design flow
- Partners: Dolphin (F), Infineon (D, F), Infiniscale (F) IMMS (D), MunEDA (D), Philips (F), STMicro-electronics (F, I), X-FAB (D), Xyalis (F)
- subcontractors: TU Munich (D) and Uni Frankfurt/M. (D)
- October 2007 until 2010

Contributions in HONEY

- In co-operation with MunEDA and X-FAB
  - WiCkeD Configurations for new X-FAB processes below 0.35μ
  - Constraint definition for structures with bipolar devices
  - Yield optimization of IP blocks
  - Verification of yield improvement with WiCkeD
- In co-operation with X-FAB
  - Consider special custom requirements (automotive)
  - Scaling IP-blocks for new X-FAB technologies
  - Process monitoring to extract statistical data
  - Ageing models on heated and stressed wafers
Experiences with WiCkeD

- Very good support by MunEDA – Thanks!
- Initial sizing (feasible solution) is sometimes difficult
  Idea: Direct calculation with op-point driven method
- Optimizing performances coming from transient simulation is difficult (highly nonlinear problem)
- Nice to have:
  - Export / import of parameters, constraints and performances from/into .CEZ to save them between topological changes
  - Edit Config-Pathes in Setup
  - Edit constraints and parameter boundaries, reset database in WiCkeD without leaving the program

Future Works

- Further co-operation based on a co-operation agreement between MunEDA, X-FAB and IMMS
- Setups for recent X-FAB technologies
- Testing beta versions of WiCkeD
Special Topics:

- IP Porting
- Local Variations (Analog & Digital)

About MunEDA

MunEDA provides leading EDA technology for analysis and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA's products and consulting enable customers to reduce the design times of their circuits and to maximize robustness and yield. MunEDA's solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

WiCkeD is a comprehensive and powerful software productive for interactive, manual, semi- and fully automatic analysis, sizing, design centering and yield optimization of analog and mixed-signal circuits. WiCkeD is marketed also under the trademark DesignMD®.

MunEDA was founded in 2001 and is a privately held company. The company headquarter is located in Munich, Germany.

MunEDA's sales & support channel in North America is MunEDA Inc. headquartered in Sunnyvale, CA, USA. Distributor in Taiwan is GTI Inc. (www.grandti.com.tw) and in Korea DAOU Xilicon (www.daouxilicon.com).
Special Topics

MunEDA User Group Meeting 2007
M. Pronath

Overview

• IP Porting
• Global and local process variation compared
• Parametrization, testbenches and measurements for optimization
• Optimization goals and strategies in nominal optimization
IP Porting

- IP Porting = Transfer of designs (intellectual property, IP) from one technology to another one
- Motivation
  - Creating libraries for a new process
  - Implementing one library in different versions (general, low power, …) of the same process technology
  - Discontinuing old processes, process convergence: Bringing existing products with long development cycles from different process lines/fabs together
- IP Porting often includes adapting the specification to the new process and supply voltage
- Target designs
  - Standard logic: Shrinking basically works, but statistical trade-offs become more and more important
  - Full-custom digital, analog, mixed-signal

Analog IP Porting System

- Cooperation of MunEDA + Faraday Technology Corp.
- Goal: build an automatic Analog IP Porting System for circuit designs
- The analog cell library consists of
  - a netlist in SPICE format,
  - a parameterized behavioral modeling with functional description and key parameters to the primary functions
  - parameterized layout information
- Many cells available, e.g.
  - Controlled delay lines
  - Operational amplifiers
  - …
- Tools: WiCkeD, HSPICE, Matlab/Simulink
- Process technology: UMC 90nm
Implementation

- Different cells require different optimization steps
  ⇒ Write one high-level optimization script for every cell
- Example: Controllable Delay Line

Controllable Delay Line: 7 Optimization Steps

<table>
<thead>
<tr>
<th>Optimization Plan</th>
<th>Optimization Targets</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1: MOS Characteristics</td>
<td>Transistor Sizes of Inverter (NMOS, PMOS), Threshold Voltage, Working at Saturation Region</td>
</tr>
<tr>
<td>Step 2: Anti-Jitter Design</td>
<td>Clocking Order, Rise/Fall Time Capacitance</td>
</tr>
<tr>
<td>Step 3: Reference Voltage</td>
<td>N/P Balance, Saturation Region</td>
</tr>
<tr>
<td>Step 4: Monotonic Current Sources</td>
<td>Increasing sizes by simulation results, from LSB to MSB</td>
</tr>
<tr>
<td>Step 5: De-couple compensation</td>
<td>Vrp, VIN, STG2</td>
</tr>
<tr>
<td>Step 6: Loading and Driving Capability</td>
<td>Speed 500MHz, Larger useful range for vrp, function work for each switch node</td>
</tr>
<tr>
<td>Step 7: Enlarge Operation Range</td>
<td>Vrp, VIN, STG2</td>
</tr>
</tbody>
</table>
Current Mirror: „small signal“ mismatch

\[ \Delta i = g_m \cdot \Delta v_{th} \]
\[ \sigma_{\Delta i} = g_m \cdot \sigma_{\Delta v_{th}} \]

Mismatch Influence

Biasing:
\[ I = k \frac{W}{L} (V_{gs} - V_{th})^2 \]
\[ g_m = \frac{\partial I}{\partial V_{gs}} = 2k \frac{W}{L} (V_{gs} - V_{th}) \]
\[ = 2\sqrt{k} \sqrt{\frac{W}{L}} I \]

Pelgrom’s Area Law:
\[ \sigma_{\Delta v_{th}} = \frac{A_{mm}}{\sqrt{W \cdot L}} \]

[\sigma_{\Delta i} \propto \sqrt{\frac{W}{L}} \cdot \sqrt{I} \cdot \frac{1}{\sqrt{W \cdot L}} = \frac{\sqrt{I}}{L} \]
Mismatch Tradeoffs

\[ \sigma_{\Delta i} \propto \sqrt{\frac{W}{L}} \cdot \sqrt{\frac{1}{I}} \cdot \frac{1}{\sqrt{W \cdot L}} \]

Mismatch

- Variance of \( V_{th} \) depends on device area: \( \sigma^2_{VT} = A^2_{VT} / (W \cdot L) \)
- Problem grows with scaling:
  - \( A^2_{VT} \) decreases only linearly with the minimum feature size
  - Therefore the variance of the minimum area device grows
  - Decreasing Vdd increases relative error \( \sigma_{VT} / V_{in \ RMS} \)
- Analog circuits cannot be shrunk as easily as digital ones.

Mismatch Analysis vs. Corner Analysis

- Mismatch Analysis considers local process variations (mismatch)
- Corner Analysis considers global process variations

Example: Folded cascode operational amplifier (CMOS 180nm)
- Process variations have small impact (σ/μ < 5%) on:
  - output voltage range, power consumption
  - gain, transient frequency, phase margin
  - slew rates
- Comparison: impact of mismatch and global variations:

\[
\begin{align*}
\sigma_{\text{mismatch}} : \sigma_{\text{global variations}} & = 5 : 1 \\
\text{power supply rejection ratio} & = 6 : 1 \\
\text{common mode rejection ratio} & = 350 : 1 \\
\text{input offset} & \\
\end{align*}
\]

Mismatch dominates global process variations
=> Corner Analysis considers minor effects only – use Mismatch Analysis

Parametrization Hints

Enforce equality constraints that are demanded by the circuit.

For example:

- W,L match due to structural constraints
- PDifferentialPair
- L match due to structural constraints
- NSimpleCurrentMirror

From circuit design, it’s known that the widths of this particular current mirror M3/M4 must match, too.

⇒ User input: Parametrize so that widths of M3/M4 match!
**Parametrization Hints**

Enforce equality constraints that are demanded by the circuit.

For example:

\[ M1 \quad M2 \quad M3 \quad M4 \]

\[ M3.W = M4.W \]

Gain

Matching enforced

M3.W

(=M4.W)

M3.w, M4.w independent

Using the right equality constraints makes optimization faster and yields better results!

**Parametrization Hints**

Equality constraints also apply to ratios:

The widths of M5-M8 can be optimized, but enforce the ratio \[ M5.W/M7.W = M6.W/M8.W \]!

By defining

\[ M5.W = m5w \]
\[ M6.W = m6w \]
\[ M7.W = m5w \times afac \]
\[ M8.W = m6w \times afac \]

using the three design parameters m5w, m6w, afac

\[ M5 \quad M7 \]
\[ M6 \quad M8 \]

Basic rule: If one design parameter is changed, the circuit should still work!
Testbenches and measurements for optimization

- Basic rule: If one design/statistical/operating parameter is changed, the simulation result should still be useful
- Example: Some testbenches work only when there's no offset. Use DC feedback for AC open-loop simulation. Else, even small offset will drive your circuit out of the linear region.

![Bad idea](image1)
![Much better](image2)

Parameter distance and scaling

- Parameter distance optimization tries to overfulfill all specs.
- There may be many solutions that fulfill all specs. Which one is considered to be the best? = Which one has highest "value" V?
- Ratios of scaling factors are like prices
  For example, scaling factor of phase margin = 2°, scaling factor of Slew Rate = 0.1MV/s:

<table>
<thead>
<tr>
<th>case</th>
<th>Phase margin</th>
<th>Slew rate</th>
<th>Ranking</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>45°</td>
<td>5 MV/s</td>
<td>2nd best, equal to C,D</td>
</tr>
<tr>
<td>B</td>
<td>46°</td>
<td>5 MV/s</td>
<td>best</td>
</tr>
<tr>
<td>C</td>
<td>47°</td>
<td>4.9 MV/s</td>
<td>Equal to A,D</td>
</tr>
<tr>
<td>D</td>
<td>43°</td>
<td>5.1 MV/s</td>
<td>Equal to A,C</td>
</tr>
<tr>
<td>E</td>
<td>46°</td>
<td>4.9 MV/s</td>
<td>worst</td>
</tr>
</tbody>
</table>

- $\Delta V = \Delta f / s$
- Lower scaling factor $\Leftrightarrow$ more important
Parameter distance and scaling

- But: Constant scaling doesn't consider the spec. Improving a performance that's close to its bounds is more valuable than improving a performance that already overfulfills the spec a lot.

\[ \Delta V = \Delta f / s \cdot \exp( -(f-f_L)/s ) \]

- This effect is also considered in parameter distance:

Special performances

- CMRR, PSRR: They are calculated from AC simulation results

\[
\text{CMRR} = -20 \cdot \log_{10}( \left\| A_{CM}/A_D \right\| )
\]

\[
\text{PSRR} = -20 \cdot \log_{10}( \left\| A_{PS}/A_D \right\| )
\]

where \( A_{CM}, A_D, A_{PS} \) are the complex common mode gain, differential gain, power supply gain, at 0Hz.

- For many circuits, the real parts of \( A_{CM} \) and \( A_{PS} \) depend nearly linearly on the process parameters and can be positive or negative with a mean value close to 0.

- The magnitude operator \( \| \cdot \| \) and the \( \log_{10} \) create a strong nonlinearity and infinite values around the mean value (\( \log_{10}(0) = -\infty \)).

- Hence: Don't optimize or analyze CMRR and PSRR, instead look at

\[
\text{re\_cmrr} = \text{Re}(A_{CM}/A_D)
\]

\[
\text{re\_psrr} = \text{Re}(A_{PS}/A_D)
\]

Transform Specs: \( \text{CMRR}>60\text{dB} \iff -0.001 < \text{re\_cmrr} < +0.001 \)
Speed up nominal optimization (1)

• Try optimizing in a sequence, for example
  – Avoid optimizing the slew rate of an instable amplifier; fix AC phase margin first, then look for the transient simulation to save simulation time.
  – Optimize at typical operating conditions first, then include operating range.

• Reduce the number of design parameters, for example
  – Try keeping all lengths at their initial values, optimize only widths.
  – Deselect capacitors for feasibility and pure DC optimizations.
  – Deselect parameters that affect only parts of the circuit that are not relevant for the current optimization step.

Speed up nominal optimization (2)

• Focus on difficult performances
  – Try to find which specs exclude each other.
  – Find influential parameters in sensitivity analysis and run parameter sweeps.

• Enabling the options „adaptive sensitivity calculation“ and „sensitivities always on worst-case conditions“ slows down, but may find a solution where the default settings don’t.
  – Run at first without these options.
  – Enable them if the first run fails.

• Apply different algorithms
  – Least squares stops automatically as soon as the specs are fulfilled, parameter distances spends more time on overfulfilling.
  – Use least squares for the first runs in a sequence, parameter distances for the last runs.
Speed up Yield Optimization

- Use parameter screening on process and mismatch parameters before YO.
- Final Monte Carlo: If parameter screening was used, then
  - **Put one simulation after the YO. Copy its design parameter values from the data display (right mouse button: pop-up menu „Copy“)**
  - **Put the Monte Carlo node before the screening node. Paste the design parameters in the Data Window.**
- Use nominal optimization with parameter distance and operating range before YO.

Thank You!