DATASHEET

MunEDA WiCkeD™ Interface to: Cadence® Virtuoso® Analog Design Environment and Cadence® Virtuoso® Multi-Mode Simulation with Spectre® Circuit Simulator and UltraSim® Full-Chip Simulator

WiCkeD™ Tools Suite

Design for Yield - WiCkeD DFM-DFY Tools Overview

WiCkeD is a comprehensive and powerful software tool suite for analysis, modelling, optimization and verification of analog and mixed-signal circuit designs.

WiCkeD supports the circuit designer with interactive manual, semi- and full-automatic tools to improve and optimize integrated circuits for functionality, performance, robustness and yield.

FEATURES

WiCkeD includes tools and methodologies for

- Topology Analysis & Constraint Management
- Specification-driven Performance Analysis & Optimization
- Response Surface Modelling
- Yield & Robustness Analysis & Optimization

WiCkeD can be operated either through a graphical user interface or a programmable scripting interface (batch mode).

THIRD PARTY SUPPORT

WiCkeD is integrated in and supports the main commercial circuit design environments and simulators including Cadence, Synopsys®, Mentor Graphics®.

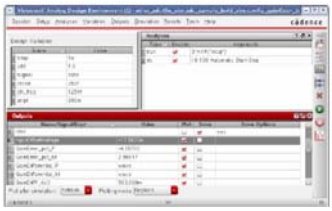
WiCkeD™ Interface to Cadence Virtuoso Custom IC Design Platform

WiCkeD fully integrated into Cadence Virtuoso platform

WiCkeD ideally complements the Cadence Virtuoso Analog Design Environment and is seamlessly integrated into both .cdb and open access versions. This enables the designer to access and utilize all WiCkeD tools easily from the familiar Cadence Virtuoso based design environment.

WiCkeD Interface to Cadence Virtuoso Analog Design Environment

WiCkeD can be started directly from the Virtuoso Analog Design Environment Tools menu with fully automated annotation of the design data from and back-annotation to schematic & netlist.



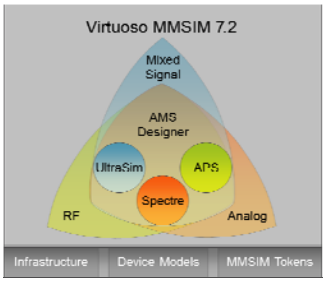
Start WiCkeD directly from ADE Tools Section

WiCkeD Interface to Cadence Virtuoso Schematic Editor

WiCkeD directly annotates the design and hierarchy data from the Cadence Virtuoso Schematic Editor followed by a fully automatic parameterization of schema-tic and netlist design parameters as well as constraint setup and editing. Specifications for circuit analysis and optimization can be easily entered in the WiCkeD Constraint Editor. Parameterized devices and hierarchies can be highlighted from WiCkeD Constraint Editor directly in the schematic editor. The technology setup (nominal, corner, mismatch, global statistics) will be done automatically from the pdk using a technology based configuration file.

WiCkeD Constraint Editor: Management of Constraints, Parameters, Performances, Specifications

WiCkeD Interface to Cadence Virtuoso Multi-Mode-Simulation



Cadence Virtuoso Multi-Mode Simulation

WiCkeD fully supports industry standard simulator Spectre Circuit Simulator and UltraSim Full-Chip Simulator. A part of Virtuoso Multi-Mode-Simulation solution.

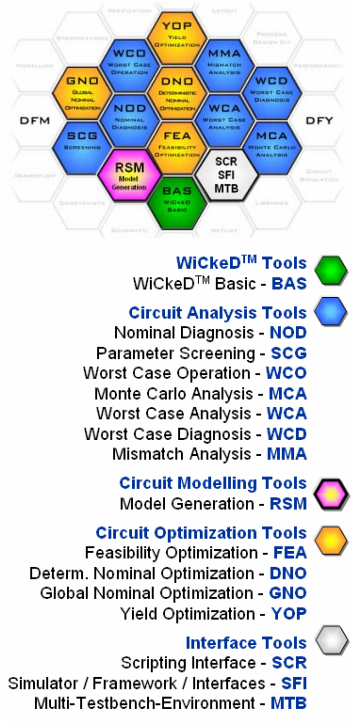
WiCkeD simulation environment interface to Cadence Multi-Mode Simulation with Spectre Circuit Simulator, UltraSim Full-Circuit Simulator

Using third party SPICE from your Cadence Virtuoso environment is also supported by the WiCkeD simulator interface environment.

WiCkeD OVERVIEW

TOOLS TO IMPROVE CIRCUIT PERFORMANCE AND YIELD

WiCkeD offers several tools for enhanced circuit analysis, modelling, optimization and verification. These tools enable customers to reduce the design times of their analog and mixed-signal circuits and to maximize robustness, reliability and yield.



MunEDA WiCkeD Tools Overview

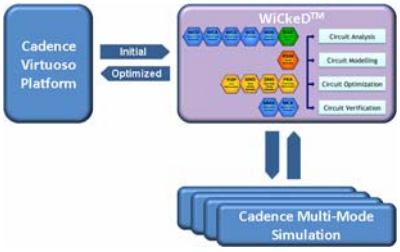
Starting with a basic design history WiCkeD delivers a powerful basic feature compilation to enable the circuit designer to do enhanced topology analysis, constraint setup and management as well as different analysis types for circuit performance, parameter sensitivity and correlation within a well documented project.

Based on this the enhanced WiCkeD tools for circuit analysis, optimization, modelling and verification can be used by the designer to check and improve the circuit functionality, performance and yield in the desired operating environment.

VIRTUOSO-WiCkeD DESIGNFLOW

INDUSTRY-PROVEN DESIGN & SIZING ENVIRONMENT

WiCkeD is seamlessly integrated into Cadence Virtuoso platform and has a tight interface with Cadence Multi-Mode simulation solution.



Cadence Virtuoso Platform & WiCkeD Designflow

A user of WiCkeD typically fulfils 6 steps to analyze and optimize a circuit starting from Cadence Virtuoso platform and Multi-Mode Simulation Environment:

- STEP 1 -- Select DUT in Virtuoso Schematic Editor
- STEP 2 – Define outputs in Virtuoso Analog Design Environment
- STEP 3 – Start WiCkeD from Virtuoso ADE Tools menu.
- STEP 4 – Set parameters, performances (outputs) and constraints in WiCkeD Constraint Editor
- STEP 5 – Analyze, model and optimize your circuit with WiCkeD and verify the results with WiCkeD and Cadence Multi-Mode Simulation.
- STEP 6 – Automatically back-annotate results from WiCkeD to netlist or schematic and continue with Cadence layout generation tools

MunEDA in Cadence Connections

MunEDA has been a member of the Cadence Connections Partner Program since 2004.

APPLICATIONS

- IC Performance & Yield Analysis and Optimization
- IP Porting & Reuse
- IP & Technology Migration
- Supports Fab Migration & Fab Light Strategies
- Supports Transistor-Level and System-Level Circuit Design

CUSTOMER BENEFITS

- Reduce design time & effort and improve design quality significantly
- Detect design failures before tape-out and going to fab
- Avoid expensive respins & redesigns, reduce fab-runs
- Achieve high yield and profits

SPECIFICATIONS

WiCkeD INPUTS/OUTPUTS

- Virtuoso Spectre Circuit Simulator netlist format
- Technology Data – PDK Process Design Kit
- Optimized netlist/schematic
- Generated behavioural models for system-level optimization

PLATFORM SUPPORT & FEATURES

- Linux, SUN Solaris®
- Documented API (C++, Tcl/Tk, Phyton, etc.)
- Export/Import Interfaces (Matlab, R, SPlus, VerilogA, VHDL-AMS)

SUPPORT & SERVICES

Cadence

For support of mentioned Cadence products please contact Cadence with www.cadence.com.

MunEDA

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