DATASHEET

MunEDA WiCkeD™ Interface to:
Synopsys® HSPICE® Circuit Simulator
Synopsys® Galaxy Custom Designer™ SE Schematic Editor

WiCkeD Tool Suite

Design for Yield - WiCkeD DFM-DFY Tools Overview

WiCkeD is a comprehensive and powerful software tool suite for analysis, modelling, optimization and verification of analog and mixed-signal circuit designs.

WiCkeD supports the circuit designer with interactive manual, semi- and full-automatic tools to improve and optimize integrated circuits for functionality, performance, robustness, and yield.

Features

WiCkeD includes tools and methodologies for

- Topology Analysis & Constraint Management
- Specification-driven Performance Analysis & Optimization
- Response Surface Modelling
- Yield & Robustness Analysis, Diagnosis, and Optimization

WiCkeD can be operated either through a graphical user interface or a programmable scripting interface (batch mode).

Third Party Support

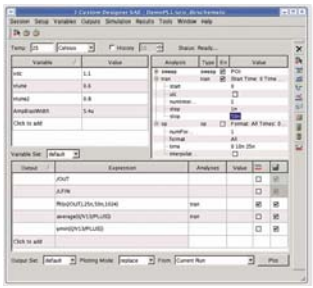
WiCkeD is integrated in and supports the main commercial circuit design environments and simulators including Synopsys®, Cadence®, Mentor Graphics®, others.

WiCkeD™ Interface to Synopsys® Custom Designer SE™

WiCkeD ideally complements the Synopsys Custom Designer SE Schematic Editor Environment. This enables circuit designers to access and utilize all WiCkeD tools intuitively from the familiar Synopsys-based design environment.

WiCkeD Interface to Synopsys Custom Designer SE Schematic Editor

WiCkeD can be started directly from the Synopsys Custom Designer Tools menu with fully automated retrieval of the design data from and back-annotation to schematic & netlist*.



Start WiCkeD directly from Custom Designer SE

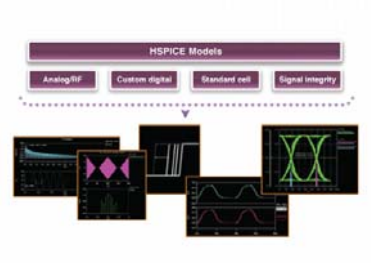
WiCkeD directly retrieves the design and hierarchy data from the Synopsys Custom Designer Schematic Editor or netlister followed by a fully automatic parameterization of schematic and netlist design parameters as well as constraint setup and editing. Specifications for circuit analysis and optimization can be easily entered in the WiCkeD Constraint Editor.

Parameterized devices and hierarchies can be highlighted from WiCkeD Constraint Editor directly in the schematic editor. The technology setup (nominal, corner, mismatch, global statistics) will be done automatically from the pdk using a technology based configuration file.

WiCkeD Constraint Editor: Management of Constraints, Parameters, Performances, Specifications

WiCkeD Interface to Synopsys HSPICE Simulation Environment

WiCkeD fully supports Synopsys HSPICE circuit simulator from Synopsys Custom Designer, netlist stand-alone as well as from third-party design environments.



Synopsys HSPICE Circuit Simulation

WiCkeD is fully compatible with HSPICE Design-for-Yield Process and Interconnect Variation Analysis, supporting the Variation Block and many other features of HSPICE.

WiCkeD simulation environment interface to Synopsys HSPICE simulation environment

* intended flow currently under implementation

WiCkeD OVERVIEW

Tools to improve circuit design performance and yield

WiCkeD offers several tools for enhanced circuit analysis, modelling, optimization, and verification. These tools enable customers to reduce the design times of their analog and mixed-signal circuits and to maximize robustness, reliability, and yield.

WiCkeD™ Tools
WiCkeD™ Basic - **BAS**

Circuit Analysis Tools
Nominal Diagnosis - **NOD**
Parameter Screening - **SCG**
Worst Case Operation - **WCO**
Monte Carlo Analysis - **MCA**
Worst Case Analysis - **WCA**
Worst Case Diagnosis - **WCD**
Mismatch Analysis - **MMA**

Circuit Modelling Tools
Model Generation - **RSM**

Circuit Optimization Tools
Feasibility Optimization - **FEA**
Determ. Nominal Optimization - **DNO**
Global Nominal Optimization - **GNO**
Yield Optimization - **YOP**

Interface Tools
Scripting Interface - **SCR**
Simulator / Framework / Interfaces - **SFI**
Multi-Testbench-Environment - **MTB**

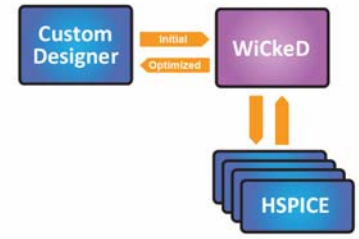
MunEDA WiCkeD Tools Overview

Starting with a basic design history WiCkeD delivers a powerful compilation of basic features that enables the circuit designer to do enhanced topology analysis, constraint setup and management, Furthermore, it includes different analyses for circuit performance, parameter sensitivity and correlation within a well documented project. Based on this the advanced WiCkeD tools for circuit analysis, optimization, modelling, and verification can be used by the designer to check and improve the circuit functionality, performance, and yield in the desired operating environment.

Synopsys-based WiCkeD Designflow

Industry-proven design & sizing environment

WiCkeD is seamlessly integrated into Synopsys Custom Designer and has a tight interface with Synopsys HSPICE simulation environment.



Designflow Synopsys Custom Designer, Synopsys HSPICE & MunEDA WiCkeD

A user of WiCkeD typically performs only six steps to analyze and optimize a circuit starting from Synopsys Custom Designer & HSPICE simulation environment:

- STEP 1 -- Select DUT in Custom Designer Schematic Editor
- STEP 2 – Define outputs in Custom Designer
- STEP 3 – Start WiCkeD from Custom Designer Tools menu
- STEP 4 – Set parameters, performances (outputs) and constraints in WiCkeD Constraint Editor
- STEP 5 – Analyze, model and optimize your circuit with WiCkeD and verify the results with WiCkeD and HSPICE
- STEP 6 – Automatically back-annotate results from WiCkeD to netlist or schematic and continue with Synopsys layout tools

MunEDA in Synopsys Partner Programs

MunEDA is member of the Synopsys in-Sync™ Program and the HSPICE integrator program.

APPLICATIONS

- IC performance & yield analysis, modelling, and optimization
- IP porting & reuse
- IP & technology migration
- Supports fab migration & fab light strategies
- Supports transistor-level and system-level circuit design

CUSTOMER BENEFITS

- Reduce design time & effort and improve design quality significantly
- Detect design failures before tape-out and going to fab
- Avoid expensive respins & redesigns, reduce fab-runs
- Achieve high yield and profits

SPECIFICATIONS

WiCkeD Inputs/Outputs

- Synopsys HSPICE netlist format
- Technology Data – PDK process design kit
- Optimized netlist/schematic
- Generated behavioural models for system-level optimization

Platform Support & Features

- Linux, SUN Solaris®
- Documented API (Tcl/Tk, Phyton)
- Export/Import Interfaces (Matlab, R, SPlus, VerilogA, VHDL-AMS)

SUPPORT & SERVICES

Synopsys

For support of mentioned Synopsys products please contact Synopsys with www.synopsys.com.

MunEDA

Get support directly from MunEDA GmbH & MunEDA Inc. or from MunEDA certified worldwide distribution & support partners. For contact directions please select www.muneda.com and info@muneda.com.