Introduction to Gilbert Cell Mixer

Circuit Description:
- Gilbert Cell mainly consists of 3 differential pairs
- Small RF signal is applied to M5,M6
- Large LO signal is applied to M1,M2 and M3,M4
- By turning M1,M2 and M3,M4 on and off the RF signal is mixed to the intermediate frequency (IF)
- Advantages: LO and RF are both balanced, good port-to-port isolations, high intercept points
- Disadvantages: high LO level required, high power supply

Example Circuit, initial sizing and simulation results

Example Circuit & Initial Sizing:
- CMOS mixer based on Gilbert Cell topology
- it consists of:
  - the Gilbert Cell
  - a current mirror
  - resistors and capacitors
- all NMOS transistors
- input resistors (R5, R6)
- source resistors (R3, R4)
- input resistors (R5, R6)
- a current mirror

Testbench:
- The testbench consists of:
  - the mixer DUT
  - three baluns
  - ports and sources
- Frequencies
  - IF = 2.5 GHz
  - LO = 2.75 GHz
  - RF = 250 MHz
- Sources
  - Vdc = 2.5 V
  - iob = 600 µA

Wiced Contraint Setup, Analysis and Optimization Flow*

Step 1 - WickeD Constraint Editor Settings:
- Design and Op. Parameters:
  - temp: from 20 °C up to 50 °C
  - vdd: from 2.4 V up to 2.5 V
- Constraints:
  - rns for differential pair
  - M5, M6 is disabled
- Performance specifications:
  - conversion gain = 8 dB
  - noise figure < 13 dB
  - power consum. < 50 mW

Step 2 - Simulation & Feasibility Optimization:
- Simulation Results:
  - two performance specifications (conversion gain and noise figure) are not fulfilled
  - after a Screening the parameters
  - L_Rin and W_Rin are removed due to this limitation no full optimization of the mixer is available with IC5.1 and WickeD 5.0

Step 3 - Nominal Optimization:
- Conversion gain and noise figure are outside the specification bounds due to this limitation no full optimization of the mixer is available with IC5.1 and WickeD 5.0

Step 4 - Worst-Case Analysis:
- Yield after Nominal Optimization between 79% and 100%
- Improvement is necessary

Step 5 - Yield Optimization & Monte-Carlo Verification:
- Yield can be increased up to 100% (WCD > 35) after 4 iterations
- Monte Carlo Analysis confirms the results of the Yield Optimization

Analysis and optimization of a CMOS mixer circuit with WiCkeD

Challenges of Mixer Optimization

There are very special challenges for the optimization of a mixer circuit. One is that special RF analyses are required, e.g. Periodic Steady State analysis (PSS) and Periodic Small Signal analyses. Another one is the application of OCEAN post processing functions to calculate mixer performances, like noise figure or intercept points.

MunEDA DFM-DFY Tool Family WiCkeD

MunEDA offers numerous tools for circuit analysis, diagnosis and circuit optimization as well as interfaces to industrial standard and inhouse design environments and simulators.

Example:

- All selected performances fulfill the specification
- Yield can be increased up to 100%
- Special RF analyses and OCEAN postprocessing functions can be used with WiCkeD
- The complete characterization and optimization of a mixer circuit requires multiple testbenches/multiple analyses of the same type

About MunEDA

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